D D WEBSTER ELECTRONICS PTY LTD
17 MALVERN STREET, BAYSWATER 3153, AUSTRALIA
Telephone: 729 8444 Telex: 36251

SPECTRUM ELEVEN
HARDWARE MANUAL

VERSION 2

This manual was supplied in conjunction with

SPECTRUM ELEVEN computer serial no.

Dated: September, 1982

WEBSTER ELECTRONICS

This manual describes only the components applicable to the 'SS' Series SPECTRUM ELEVEN Computers. Information on the 'SP' Series Spectrum Eleven computers can be found in the original Spectrum 11 Users Manual, issued December, 1978.

Issued in conjunction with this hardware manual is the Spectrum Eleven RT-11 Software Manual.

Each member of the Spectrum Eleven family was conceived as a system rather than a set of components. All of the common interface requirements of Commercial, Educational, Industrial, and Scientific applications have been merged into one composite General Purpose Multiple Interface, or GPMI.

At the heart of the GPMI is a microprogrammed I/O processor which operates concurrently with the LSI-11 central processor to assist with data input and output operations.

The GPMI provides its own high speed direct memory access connection to the Winchester and Floppy disks allowing transfer rates many times greater than the limiting bandwidth of the Q-bus. DMA efficiency is further enhanced by avoiding CPU and bus latencies.

The GPMI arbitrates all contentions for device and memory access, and handles dynamic memory refresh. It continuously polls all devices for interrupt requests, and arbitrates and manages the interrupt process.

Component count, interconnection count, and power dissipation are all better than halved by generalising and combining the interface logic, so improving reliability over discrete interface designs.

The GPMI I/O processor removes the burden of I/O housekeeping from the LSI-11 central processor, freeing it for its primary function of fetching and executing useful instructions. The presence of the GPMI is transparent to programs running in the LSI-11, and imposes no significant overhead on normal program execution.

The GPMI takes only one backplane slot and one bus load, and consists of 2 or 3 circuit boards linked by flat cable. Each circuit board used in the assembly of the GPMI has been designed with individual characteristics and consequently certain restrictions do apply in the creation of the interface set. The GPMI is created with a mandatory 'S' board, a choice between a 'B' or 'M' board and can include a 'T' board. This is completely dependent on storage device requirements.

In systems with parity memory, that is systems with a memory capacity greater than 256Kb, the 'S' board is replaced with a 'Y' board and either one or two 'X' boards. These boards perform the same basic function as the 'S' board but allow for a greater memory capacity, and with the addition of a parity bit per byte of storage, provide a memory error detection scheme.

Explicit details on the GPMI components can be referenced in the Engineering Section of this manual.

INTRODUCTION

The Spectrum Eleven family comprises a series of powerful and extremely compact disk computers which form the basis of systems for various applications. The machines are based on Digital Equipment Corporation (DEC) LSI-11/2 or LSI-11/23 processors with a wide range of storage devices, memory options, terminals, and printers available. All future upgrades will be compatible with existing family members and as requirements change, hardware may be added or substituted.

All Spectrum Eleven computers are supplied complete with:

- Two EIA serial line controllers, extended to rear panel
- One CENTRONICS-compatible line printer interface
- Automatic firmware bootstrap
- Line time clock

Configuration options include:

- 64/128/256/512Kb, 1Mb, or 2Mb MOS memory
- Parallel Card Reader controller
- Additional spare backplane slots
- Dual 0.315 megabyte floppy disks
- Single or dual 1.26 megabyte 8" floppy disks
- RK05 compatible 20 megabyte 14" cartridge disk
- RK06 compatible 8.5 megabyte 8" fixed Winchester disk
- RK07 compatible 30 megabyte 8", 56 or 132 megabyte 14" fixed Winchester disk
- TM11 compatible 1600 BPI 1/2" streaming magnetic tape
- Additional serial lines

Packing options:

- Desk-top cabinet
- Floor console
- Work station
- Rack mount
- Lockable front desk-top cabinet

For explicit details on Spectrum Eleven configurations, refer to the specifications in the chapters following.

2.1 LSI-11 PROCESSOR

The DEC LSI-11, a 16-bit architecture, incorporates the following main features:

More than 400 executable instructions;

Extensive computer power and small physical size;

Direct addressing of 64K 8-bit bytes;

Optional memory mapping to 256 kilobyte;

Efficient handling of 8-bit characters without the need to rotate or mask;

Asynchronous bus allows the processor and system components to run at the highest possible speed;

Hardware sequential memory manipulation facilitates the handling of structured data, subroutines and interrupts;

Direct memory access for multiple devices;

8 general purpose registers for accumulators or address generation;

Priority-structured I/O interrupt system;

Vectored interrupts.

2.2 GPMI INTERFACE

All memory, bootstrap, disk, terminal, printer and card reader electronics have been merged to form one composite interface with all functions under the direction of a microprogrammed controller.

The GPMI controller is responsible for all bus transfers between the bus and the devices, including memory, and from device to device, as in direct memory access.

It simulates the peripheral registers of all devices with RAMS and multiplexers, and manages the incrementing of the simulated transfer count and memory address registers for the DMA devices;

It performs DMA internally, enhancing throughput by avoiding CPU and bus latencies;

It generates all of the peculiar timing waveforms and clocks required by the highly diverse devices, simply as a sequence of microprogrammed steps;

It polls all devices at 8MHz for interrupt requests and handles the refresh cycles for the dynamic memory;

It arbitrates all contentions for memory and device access.

2.3 SPECTRUM ELEVEN MEMORY ORGANISATION

Spectrum models can be supplied with 64 kilobyte through 2 megabyte of 16-bit read/write memory. Not all of the memory is directly addressable as a sector must be left free at the top of the 16-bit addressing space of the LSI-11 to accommodate the peripheral registers. The size of this sector is 4 kilobytes for models supplied with 64 kilobytes of main memory and 8 kilobytes for models with more than 64 kilobytes of main memory. The remaining memory space can be accessed in two ways. The DMA devices, including the Iterator, can access the memory behind the I/O page as well as all of main memory. Secondly, a Spectrum 11/23 with memory management can access all memory except the page behind the I/O page.

2.4 SPECTRUM ELEVEN DISKS

Spectrum machines can be configured with floppy disks, cartridge disk, cartridge disk with floppy disks, Winchester disk, or Winchester disk with floppy disk (or magtape). Details of available models can be referenced in the next chapter.

Pertinent facts on these disk types are related in the subsequent paragraphs.

2.4.1 Floppy Disks

Floppy disks are incorporated in Spectrum machines as re-usable, inexpensive and compact recording media. They are made from polyester film coated with magnetic oxide and for protection during operation, handling and storage, are enclosed in a flexible plastic envelope. In operation the disk rotates at 360 rpm while a magnetic read/write head accesses the disk surface via a radial slot in the envelope.

High performance is ensured by use of a fast steel belt head positioner, spiralled index formatting, and direct memory access data transfer. High capacity can be achieved by use of a proprietary large sector, double sided, double density diskette format.

Built-in automatic format sensing optionally permits reading and writing of Universal Interchange diskettes, allowing totally flexible access to DEC RX01, IBM 3740, and 8-inch CP/M systems. Fully accommodated also are the Spectrum 1S, 1D and 2D formats.

2.4.2 Cartridge Disk

A 20 megabyte, DEC RK-11 compatible, cartridge disk provides medium rated disk performance and improved storage capacity for a Spectrum Eleven. The removable volume is 5 megabyte and the fixed 15 megabyte of disk is conveniently sectioned into three platters.

Data are stored serially in concentric tracks on both surfaces of the disk.

2.4.3 Winchester Disk

A series of four high performance Winchester disks, fully compatible with DEC RK06 or RK07 systems, provide a formatted capacity of 8.5 megabyte and 29.5 megabyte respectively for the 8-inch disks, and 56 megabyte and 132 megabyte respectively for the 14-inch disks. For the latter two sizes, an internal switch setting permits their use as fully contiguous file space, or mapped into 2 or 4 RK07 software compatible units.

The non-removable shock mounted head/media assemblies are fully sealed against external contaminants such as dust, grit, lint, and smoke particles, thus eliminating the major cause of head crashes in more conventional disk designs. Long term reliability and data integrity of this class of disk drive are without compare.

Disk access performance is optimised in most models by use of high-energy voice coil head positioners while the slightly slower model (8.5 megabyte) employs a stepping motor. Rotational latency is minimised by use of a 3100 rpm (14-inch drive) or 3600 rpm (8-inch drive) brushless direct drive spindle motor. Instantaneous data transfer rates, approaching one megabyte per second (8-inch drives) and exceeding one megabyte per second (14-inch drives), are preserved direct to memory by use of an independent memory bus and transparent I/O processor. The GPMI system is fast enough to take full advantage of the speed of the Winchester disk whereas the Q-bus is too slow to handle the transfer rate without resorting to time-consuming and expensive techniques such as full sector buffering.

Removable backup storage is provided by a magnetic tape and/or floppy disk sub-system.

2.5 SPECTRUM ELEVEN MAGNETIC TAPE

Removable backup storage is provided for the 14-inch Winchester disks by an auto-threading 1/2-inch ANSI compatible magnetic tape drive. The storage capacity ranges from 4 megabyte (600 foot, 512 byte blocks) to a maximum of 40 megabyte (2400 foot, 8 Kbyte blocks). The drive functions in either large-block streaming mode for rapid disk image copying, or in stop-start mode for TM11 compatible file oriented operations.

2.6 NON-SPECTRUM INTERFACES

The backplane of the Spectrum Eleven is Q-bus compatible. Most independently sourced Q-bus interfaces (with the exception of memory) can be used in the Spectrum backplane.

INTRODUCTION

The general specifications for Spectrum Eleven computers conform to this summary, with variants between models stated where applicable. In addition, the remaining chapters in this section provide more detailed specifications for each model type.

PROCESSOR	DEC LSI-11/2 or LSI-11/23
INSTRUCTION SET	PDP-11 compatible
MEMORY	MOS 64/128/256/512Kb, 1Mb, or 2Mb
MEMORY PARITY	Implemented on models with more than 256Kb of memory
BOOTSTRAP	Bipolar PROM, 512 bytes
LINE TIME CLOCK	50/60 Hz interrupt
ASYNCHRONOUS SERIAL LINES	2, DLV11 compatible, 50 - 9600 baud Expandable to 22 maximum
LINE PRINTER INTERFACE	LPV11 compatible, Centronics pinouts
CARD READER INTERFACE	DMA (model B only), Peripheral Dynamics pinouts
EXPANSION	LSI-11 bus compatible, 4 or 6 slot quad capacity. See Backplane Configurations (Section 2) for details.
DIMENSIONS	Desk-top cabinet models (Package 0) 22cm high, 48cm wide, 50cm deep (8.75" x 19" x 20") Floor console models (Package 1) 70cm high, 57cm wide, 75cm deep (27.5" x 22.5" x 29.5")

NET WEIGHT (approximate)

Desk-top models:	Models B and D	32Kg (70lbs)
	Models GC and HC	35Kg (77lbs)
Console models:	Model JM	104Kg (229lbs)
	Model KM	103Kg (227lbs)
	Model GCM	90Kg (198lbs)
	Models DP and BP	113Kg (249lbs)
	Model P	100Kg (220lbs)
Rack Mount modules:	Models B and D	29Kg (64lbs)
	Models GC and HC	32Kg (71lbs)

POWER REQUIREMENTS

105-205 volt 10 amp 50/60 Hz
210-250 volt 5 amp 50/60 Hz
General purpose standard power outlet

3.1 CONFIGURATION OPTIONS

There are ten basic model types available, not taking into account the memory or processor options.

LSI-11/2 PROCESSOR	LSI-11/23 PROCESSOR with Memory Management
SS11B3	
SS11B4	
SS11D3	SS23D3
SS11D4	SS23D4
	SS23D5
	SS23D6
SS11GC2	SS23GC3
SS11GC4	SS23GC4
SS11GC3	SS23GC5
	SS23GC6
SS11GCM2	SS23GCM3
SS11GCM4	SS23GCM4
SS11GCM3	
SS11HC2	SS23HC3
SS11HC3	SS23HC4
SS11HC4	SS23HC5
	SS23HC6
SS11JM2	SS23JM3
SS11JM3	SS23JM4
SS11JM4	SS23JM5
	SS23JM6
	SS23JM7
SS11KM2	SS23KM3
SS11KM3	SS23KM4
SS11KM4	SS23KM5
	SS23KM6
	SS23KM7
SS11BP2	
SS11DP2	SS23DP3
	SS23DP4
SS11P2	SS23P3
	SS23P4

3.1.1 Definition of Codes

Typical Code Number

```
                    SS23  GC  4
                    ----  --  -
                       ^
Processor option -----¦   ^
Storage option   ---------¦   ^
Memory option    ------------¦
```

Processor Options

SS11 LSI-11/2 with iterator.
Operates under RT-11 and can include TSX.

SS23 LSI-11/23 with memory management and iterator.
Operates under RT-11 and can include TSX-Plus.

Storage Options

B Dual 315 kilobyte floppy disk (630 kilobyte on-line)
C Single 1.26 megabyte floppy disk
D Dual 1.26 megabyte floppy disk (2.52 megabyte on-line)
P 20 megabyte cartridge disk (15 fixed, 5 removable)
G Single 30 megabyte fixed Winchester disk
H Single 8.5 megabyte fixed Winchester disk
J Single 132 megabyte fixed Winchester disk
K Single 56 megabyte fixed Winchester disk
M Single 40 megabyte 1600 BPI 1/2-inch streaming tape

Memory Options

2 64 kilobyte MOS memory
3 128 kilobyte MOS memory
4 256 kilobyte MOS memory
5 512 kilobyte MOS parity memory
6 1 megabyte MOS parity memory
7 2 megabyte MOS parity memory

FLOPPY DISK SYSTEM

Models B, C, D

Drives	2 standard, 4 with extender
Density	Single (Model B) Double (Models C and D)
Disk transfer mode	Direct Memory Access
Disk format	Software read/writeable
Media life	5 million passes per track
Media compatibility	DEC RX01/IBM, automatically sensed

FLOPPY DISK ORGANISATION

NATIVE MODE

	MODEL B	MODEL C	MODEL D
Surfaces	1	2	2
Tracks per surface	77	77	77
Sectors per track	8	16	16
Bytes per sector	512	512	512
Formatted capacity, bytes	315,392	1,261,568	2,523,136
Recording mode	FM	MFM	MFM
Recording density, BPI	3408	6816	6816
Track density, TPI	48	48	48
Media specification (ANSI)	X3B8/81-40	X3B8/81-40	X3B8/81-40
Native format type*	1S	2D	2D
Additional format capability*	DX	DX,1S,1D	DX,1S,1D

INTERCHANGE MODE

	All Models
Surfaces	1
Tracks per surface	76
Sectors per track	26
Bytes per sector	128
Formatted capacity, bytes	252,928
Recording mode	FM
Recording density, BPI	3408
Track density, TPI	48
Media specification (ANSI)	X3,73

FLOPPY DISK PERFORMANCE

	MODEL B	MODEL C	MODEL D
NATIVE MODE			
Single sector transfer rate, kilobyte/sec:	31.25	62.5	62.5
Avg multi track transfer rate, kilobyte/sec:	19.7	43.7	43.7
Head load time, millisec:	35	35	35
Track to track seek time, millisec:	3	3	3
Average access time, millisec:	324	210	210
Average seek time, millisec:	91	91	91
Maximum seek time, millisec:	246	246	246
Head setting time, millisec:	15	15	15
Avg rotational latency, millisec:	83	83	83
Spin up time, seconds:	2	2	2

	All Models
INTERCHANGE MODE (Differences only)	
Single sector transfer rate, kilobyte/sec:	31.3
Avg multi track transfer rate, kilobyte/sec:	6.7

*Format Type Definitions

		Heads	Tracks	Sectors	Bytes	Bytes/ diskette
DX	IBM/DEC Normal density	1	76	26	128	252,928
1S	WEBSTER Normal density	1	77	8	512	315,392
1D	WEBSTER 1 Head dual density	1	77	16	512	630,784
2D	WEBSTER 2 Head dual density	2	77	16	512	1,261,568

CARTRIDGE DISK SYSTEM

Model P

Drives	1 drive
Software compatibility	8 x DEC RK05
Media	15Mb non-removable, 5Mb removable

CARTRIDGE DISK ORGANISATION

Formatted capacity, kilobytes	19,955,712

CARTRIDGE DISK PERFORMANCE

Avg transfer rate, kilobytes/sec:	240
Instantaneous transfer rate, kilobytes/sec:	305.2
Track to track seek time, millisec:	10
Avg seek time, millisec:	40
Avg rotational latency, millisec:	12.5
Spin up time, seconds:	120

WINCHESTER DISK SYSTEM

Models H, G, K, J

Drives	1 drive
Software compatibility	1 x DEC RK06 (H) 1 x DEC RK07 (G) 2 x DEC RK07 (K) 4 x DEC RK07 (J)
Media	Multi-platter, fixed: Models H & G - 8 inch Models K & J - 14 inch
Head positioning mechanism	Model H - Stepping motor Models G, K, J - Voice coil

WINCHESTER DISK ORGANISATION

	MODEL H	MODEL G
Track density, TPI	180	480
Recording density, BPI (MFM)	7475	6670
Software emulation	DEC/RK06	DEC/RK07
MAPPED MODE ONLY		
Units	1	1
Cylinders	253	875
Surfaces per cylinder	3	3
Sectors per surface	22	22
Bytes per sector	512	512
Formatted capacity, bytes	8,549,376	29,568,000

	MODEL K	MODEL J
Track density, TPI	960	960
Recording density, BPI (MFM)	6430	6430
Software emulation	DEC/RK07	DEC/RK07

MAPPED MODE

Units	2	4
Cylinders per unit	840	980
Surfaces per cylinder	3	3
Sectors per surface	22	22
Bytes per sector	512	512
Formatted capacity, bytes	56,770,560	132,464,640

UNMAPPED MODE

Units	1	1
Cylinders per unit	1121	1121
Surfaces per cylinder	3	7
Sectors per surface	33	33
Bytes per sector	512	512
Formatted capacity, bytes	56,821,248	132,582,912

WINCHESTER DISK PERFORMANCE

MODEL:	H	G	K	J
Single sector transfer rate, kilobytes/sec:	900	806	1040	1040
Avg multi track transfer rate, kilobyte/sec:	447	565	655	764
Track to track seek time, millisec:	23	10	8	8
Avg seek time, millisec:	73	48	40	40
Maximum seek time, millisec:	140	90	85	75
Avg rotational latency, millisec:	8.4	8.3	9.7	9.7
Spin up time, seconds:	30	30	30	50
Stop time, seconds:	30	30	30	50

BACKUP CHARACTERISTICS

MODEL:	H	G	K	J
Diskettes required for full backup:	7	24	n/a	n/a
Operator time, minutes:	5.2	18	n/a	n/a
Magtapes required for full backup:	n/a	1	2	4
Operator time, minutes:	n/a	5	10	20

MAGNETIC TAPE SYSTEM

Model M

Units	1 unit
Compatibility	DEC TM11, software and media
Media	1/2 inch wide, 1.5 mil thick, ANSI standard X3.40-1976
Reel sizes	10.5, 8.5, or 7 inch reels (2400, 1200, or 600 foot)

MAGNETIC TAPE ORGANISATION

Format	9 track 1600 BPI phase encoded
Storage capacity	41 megabyte (2400 foot, 8 Kbyte blocks) 15 megabyte (2400 foot, 512 byte blocks) 8 megabyte (1200 foot, 512 byte blocks) 4 megabyte (600 foot, 512 byte blocks)
Rewind speed	200 inch/second average
Tape load time	30 seconds
Backup time	3.5 minutes/30 megabyte (100 IPS)

MAGNETIC TAPE PERFORMANCE

SELECTABLE TAPE SPEEDS:	25 INCH/SEC	100 INCH/SEC
Instantaneous transfer rate, kilobyte/sec:	40	160
Data access time, millisec:	40	260
Reposition time, millisec:	120	780
Read reinstruct time, millisec:	15	4
Write reinstruct time, millisec:	12	3

INTRODUCTION

If a Spectrum machine is to be delivered and installed without the supervision of Customer Service personnel, or is to be re-located at another site, please take heed of the transportation requirements specified in this chapter.

1.1 TRANSPORT SCREWS

Desk-top machines include two transport screws situated underneath the front of the cabinet. These screws are only removed to gain internal access.

CAUTION: The screws must be replaced before attempting to transport the equipment, as internal damage could result.

1.2 FLOPPY DISK HEAD PROTECTION (Models B, C, D)

Floppy disk drives are shipped with cardboard inserts installed to protect the head mechanism.

CAUTION: The inserts must be removed and retained for future use to protect the heads during transportation.

1.3 CARTRIDGE DISK HEAD RESTRAINT (Model P)

To gain internal access refer to the instructions in paragraph 3.3, then proceed as follows:

Loosen and remove the horizontal tie-down screw and rubber grommet which anchor the balance weight on the carriage assembly to the magnet assembly. The screw and rubber grommet should then be stored in the tapped hole provided on the base assembly, adjacent to the position transducer assembly.

CAUTION: If the unit is shipped, the tie-down screw and rubber grommet must be used to secure the carriage assembly. The tie-down screw must be tightened firmly but not to the point where the grommet is distorted as damage could occur to the carriage bearings.

1.4 8" WINCHESTER DISK LOCKING DEVICE (Model G only)

The locking device for this model (Model H machines do not require or possess a head restraint feature) is a lever which is placed in the locked position to restrain the heads during transportation. The 'Unlock' and 'Locked' positions are clearly marked.

To gain access to the lever, proceed as follows:

System Cabinet Models

Face the machine and remove the righthand side cover. The lever can then be accessed through the aperture at the rear of the side panel

Desk-Top Models

Remove the top cover and access the lever through the exposed opening.

CAUTION: The lever must be released from the locked position before the machine can be used, and likewise must be in the locked position before future transportation.

1.5 14" WINCHESTER DISK LOCKING DEVICE (Models K and J)

Two locking devices are present on these models (Figure 1-1). Easier access can be gained by pulling the drive out from the rear of the cabinet (refer paragraph 3.1.2).

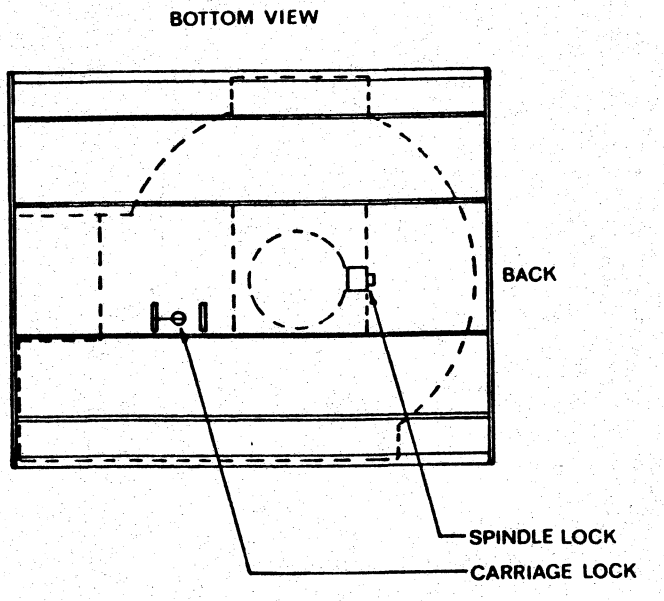


Figure 1-1

Disengage the spindle lock by moving the spindle locking lever to the 'UNLOCK' position. Disengage the carriage lock by moving the carriage locking wire loop to the 'UNLOCK' position.

CAUTION: The spindle and carriage locks must be returned to their respective 'LOCK' positions before the machine is transported.

INTRODUCTION

Spectrum Eleven installations require no special environment considerations. Normal comfortable working conditions are adequate with regard to temperature, humidity, and air cleanliness.

Air movement must not be hampered in the area of the cooling inlet fans which are located at the rear of the machine.

Systems should not be operated outside the environmental limits specified in the following paragraphs.

2.1 TEMPERATURE/HUMIDITY CONSIDERATIONS

AMBIENT TEMPERATURE	10 to 38 Celsius (50 to 100 deg F)
RELATIVE HUMIDITY	20% to 80% condensing
WET BULB TEMPERATURE	26 Celsius (78 deg F) maximum

2.2 ENVIRONMENT

ALTITUDE	30 m below to 3000 m above sea level

2.3 POWER REQUIREMENTS

Power is supplied from any normal general purpose outlet.

AC SUPPLY VOLTAGE	105-125 or 210-250 volts RMS
AC SUPPLY FREQUENCY	50 or 60 Hz

2.4 LIGHTING

If CRT devices are part of the system, the illumination surrounding these peripherals should be arranged to avoid glare from the screen.

2.5 RESTRICTIONS

Winchester disks can only operate in a horizontal position therefore, unlike the Floppy disk systems, the desk-top system cabinets do not possess the adjustable feet for front-end elevation.

INTRODUCTION

Before gaining internal access to any part of the Spectrum Eleven, it is recommended that all external connections and the power on/off key be removed.

3.1 SPECTRUM ELEVEN

3.1.1 Desk-Top Models

Place the desk-top model (Figure 3-1) on a cleared table top.

A Allow the front to overhang the edge of the table by approximately 5 cm (2") and check that a surface clearance of at least 50 cm (20") has been left behind the machine.

B Remove the two knurled transport screws from underneath the front of the cabinet.

C Unscrew the four cover screws (2 screws to each side) and remove the cover.

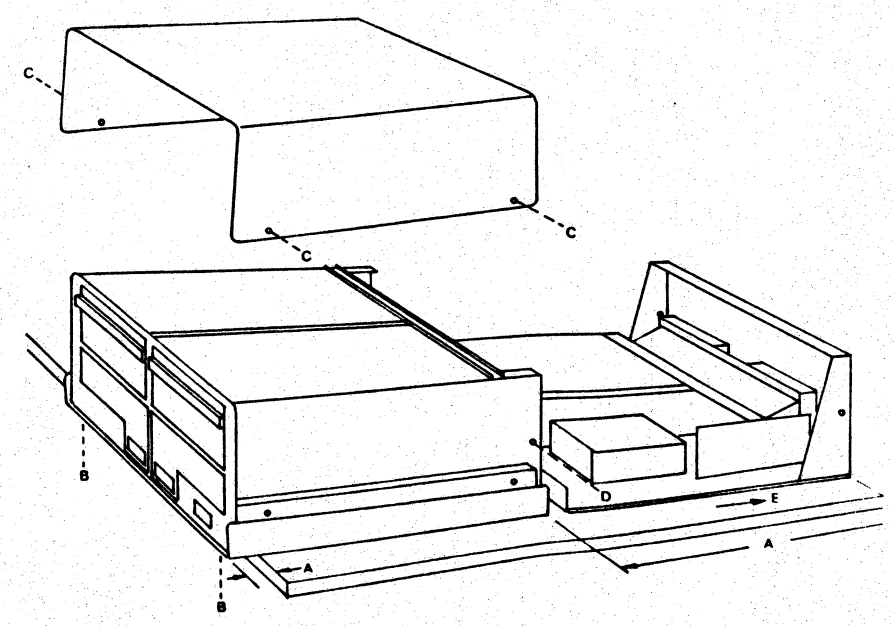


Figure 3-1

D Remove the two remaining knurled screws from the sides of the rear panel.

E Slide the internal chassis out from the rear making sure that the internal cables unfold freely and do not strain and tangle.

The chassis may then be placed on the table behind the machine and free access will be available to all internal components.

3.1.2 Console Models

Using a 1/8th inch Allan key, remove the eight screws and two side panels. Then remove the two knurled screws from the sides of the Spectrum rear panel. The internal chassis can then be slid out from the rear but ensure that the cables unfold freely.

3.1.3 Re-assembly

Reassembly for both model types consists of both sets of steps being carried out in reverse. During the process ensure that the internal cables fold freely.

It is most important that all screws be replaced, including the two front lower transport screws, as internal damage could result during subsequent transportation.

3.2 MAGNETIC TAPE UNIT

To gain access to the tape path area (illustrated in Figure 3-2) for routine cleaning, proceed as instructed (Figure 3-3).

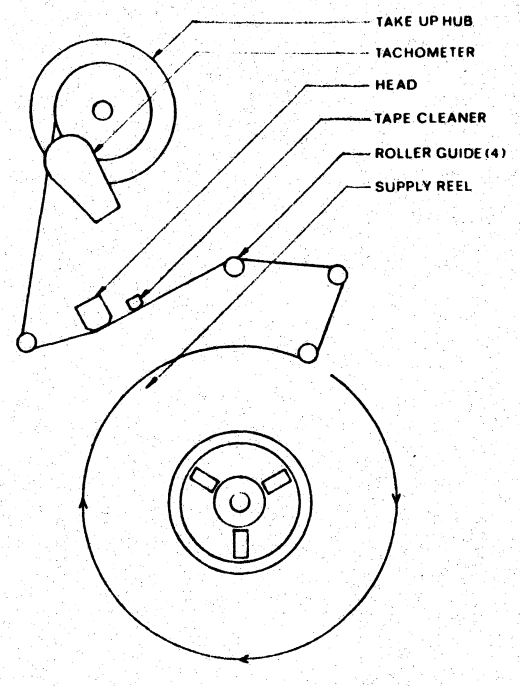


Figure 3-2

A Release rack containing mechanism located behind lower left-hand side of front panel.

B Holding front panel firmly, withdraw drive on its slides until first lock engages.

C Hold each side of top (front) cover and raise cover to its locked, retained position.

D To return drive to its operating position, close top (front) cover.

E Push unit back on slides until detent engages.

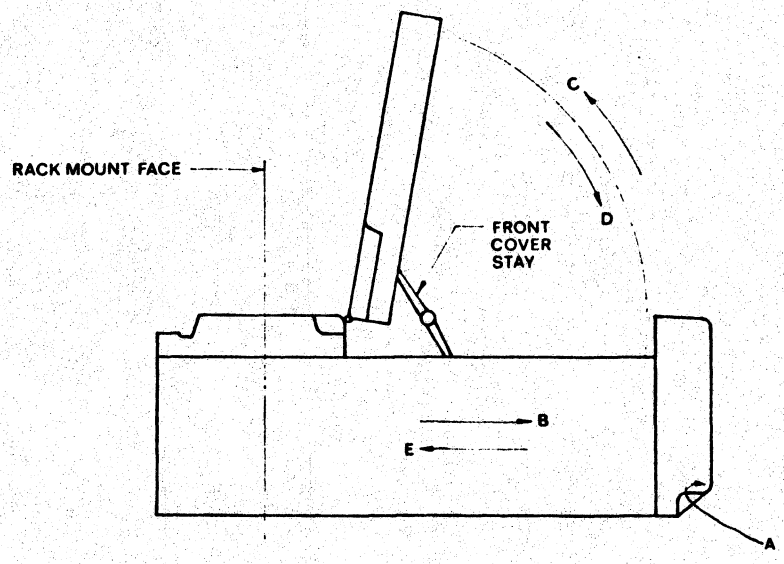


Figure 3-3

To gain access to the takeup hub area, place drive in operator maintenance position (paragraph 3.2) and proceed as follows:

A Release first lock retainer on right slide.

B Withdraw drive firmly on slides until second lock engages.

CAUTION:

When drive fully withdrawn, the tape unit may cause the cabinet to overbalance. External support is recommended.

C Raise front top cover and release retainer by removing pin from its pivot.

D Release two Ny-Latch fasteners and raise rear top cover. Secure rear top cover by placing retainer (on left side) into its retaining slot (Figure 3-4).

E Reverse process to lower top cover and return drive to its installed position.

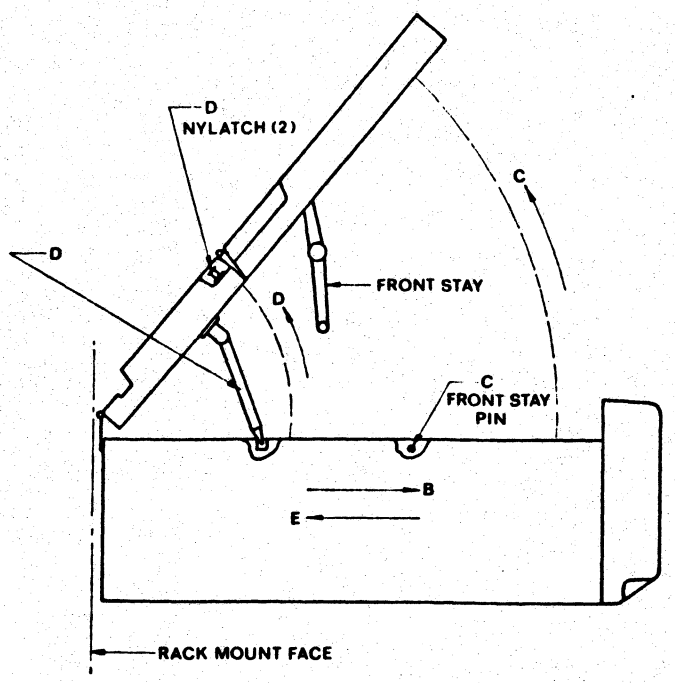


Figure 3-4

3.3 CARTRIDGE DISK

To gain internal access, proceed as follows:

1. Remove the five screws along the sides of the unit.
2. Slide the dust cover toward the rear of the unit until the front edge clears the bezel and remove the dust cover.
3. Locate and loosen the two retaining screws on top of the Logic PCB and rotate the hinged card structure up and to the rear. The spring-loaded PCB pivot lock will automatically lock the Logic PCB into a vertical position.
4. Loosen the two retaining screws which secure the Servo PCB to the Logic PCB.
5. Finally swing the Servo PCB into its extended position, and engage the locking pin and the PCB support bracket.

INTRODUCTION

Rear connectors and cables are supplied for all peripheral devices purchased as components of an integrated Spectrum Eleven system. Should a user decide to integrate his own peripheral equipment, reference should be made to the connection details specified in Chapter 5, and heed should be taken of the Warranty provisions (refer Section 6).

4.1 CONNECTIONS

All connections to the Spectrum Eleven are made from the back (Figure 4-1). Note that for JM and KM models, the connections are slightly different.

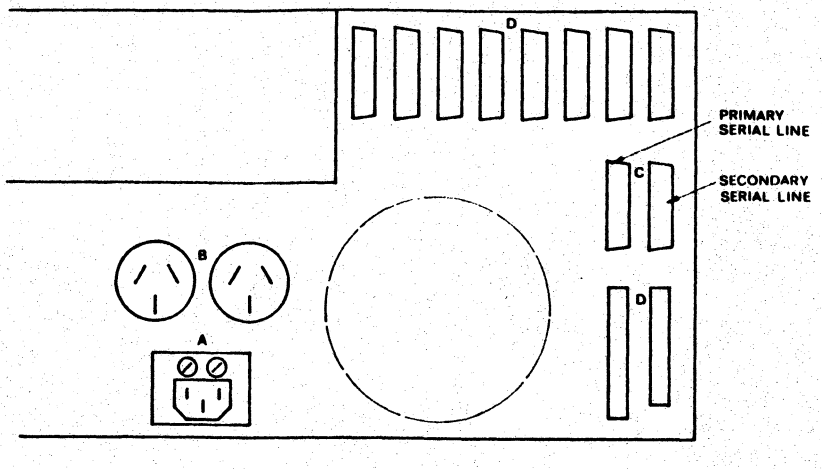


Figure 4-1

A At the bottom centre of the rear panel is the AC input connector with dual integral 5-amp fuse holders.

B Immediately above this are two general purpose AC power convenience outlets for terminals or other peripherals to a total of 3 amps maximum. These outlets are controlled by the Spectrum Eleven fuses and mains off-on switch.

C At the right of the rear panel are two 25-way standard female RS-232C connectors for terminals or other serial line connections. The inner-most of these is connected to the console or system terminal and the outer-most to any secondary serial line device that may be present.

D Several spare outlets are provided in the rear panel to accommodate additional peripheral connectors of various types. The final assignment is dependent on details of the system as integrated.

4.2 CABLE LENGTHS

To ensure reliable operation, recommended maximum cable lengths are:

Printer, flat flexible cable:		10 metre
Card Reader, flat flexible cable:		10 metre
RS-232C lines, dual twisted pairs:	300 baud	1000 metre
	1200 baud	250 metre
	1800 baud	175 metre
	2400 baud	125 metre
	4800 baud	60 metre
	9600 baud	30 metre
	19200 baud	15 metre

5.1 SERIAL LINE CONNECTIONS

20-way Internal Connector located on the 'B'/'M' Board.
(Mating connector SCOTCHFLEX 3421-3000)

Pin	Function	Pin	Function
1	ground	2	ground
3	RS-232C serial out A	4	RS-232C serial out B
5	RS-232C reader run A	6	RS-232C reader run B
7	-5V (ref only)	8	-5V (ref only)
9	+12V (ref only)	10	+12V (ref only)
11	ground	12	ground
13	ground	14	ground
15	RS-232C serial in A	16	RS-232C serial in B
17	RS-232C status in A	18	RS-232C status in B
10	+5V (ref only)	20	+5V (ref only)

25-way Rear Panel Connector RS-232C (serial lines A & B)
(Mating connector AMPHENOL 17-90250-15)

Pin	Function	
1	ground	
2	RS-232C serial in	
3	RS-232C serial out	
7	ground	
20	RS-232C status in	
5	RS-232C reader run	) These connections are made through
9	-5V (ref only)	) optional wire links on the 1538L/04
10	+12V (ref only)	) PCB. Systems are normally supplied
13	+5V (ref only)	) without the links.

DLV11 Serial Line Connections
25-way Rear Panel Connector AMPHENOL

Pin	Function
1	ground
2	RS-232C serial in
3	RS-232C serial out
7	ground

5.2 LINE PRINTER CONNECTIONS

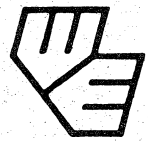
34-way Connector (all models)
(Mating Connector female SCOTCHFLEX 3414-3000)

Pin	Function	Pin	Function
1	strobe/	18	ground
2	data 1	19	ground
3	data 2	20	ground
4	data 3	21	ground
5	data 4	22	ground
6	data 5	23	ground
7	data 6	24	ground
8	data 7	25	ground
9	data 8	26	ground
10	no connection	27	ground
11	busy	28	ground
12	no connection	29	ground
13	no connection	30	prime/
14	ground	31	fault/
15	no connection	32	no connection
16	no connection	33	no connection
17	ground	34	ground

5.3 CARD READER CONNECTIONS

40-way connector (Model B)
(Mating connector female SCOTCHFLEX 4014-3000)

Pin	Function	Pin	Function
1	ground	2	zone 9/
3	ground	4	zone 8/
5	ground	6	zone 7/
7	ground	8	zone 6/
9	ground	10	zone 5/
11	ground	12	zone 4/
13	ground	14	zone 3/
15	ground	16	zone 2/
17	ground	18	zone 1/
19	ground	20	zone 0/
21	ground	22	zone 11/
23	ground	24	zone 12/
25	ground	26	ready/ (feed check status/)
27	ground	28	busy/ (card in head/)
29	ground	30	strobe/
31	ground	32	busy/ (ext card in head/)
33	ground	34	no connection
35	ground	36	pick command/
37	ground	38	no connection
39	ground	40	no connection



INTRODUCTION

When the terminals or other serial line devices have been selected for operation with the Spectrum Eleven, it is necessary to establish and set the correct baud rates and other line parameters by means of two miniature 10-bank switches located inside the machine. If the Spectrum Eleven was purchased as part of an integrated system, these switch settings will have already been made and no further attention is required. Users wishing to configure or re-configure their own systems can reference the following tables.

6.1 LINE PARAMETER SWITCH SETTINGS
(For 'M' or 'B' circuit boards only)

After gaining access to the Spectrum Eleven using the established procedure, the two miniature 10-bank switches will be seen located near the front edge of the upper logic board. The switch bank closest to the left side of the machine controls the line parameters for Serial Line A (the console terminal), while the bank nearest the centre of the machine controls the line parameters for Serial Line B. The functions of these switches are as follows:

Switch 1

For Serial Line A (the console port), switch 1 in the OFF position allows the BREAK key on the console terminal to immediately halt the processor and enter the Console ODT mode. This function is useful for machine maintenance or assembly language program development. With this switch in the ON position, pressing the BREAK key will have no effect. This is the preferred position when the machine is used primarily for turnkey applications or high level language programming.

For Serial Line B (Model B), switch 1 behaves as for Serial Line A. In Models C and D however, switch 1 of the B bank has a different function. In the OFF position it places an unconditional halt on the system bus which puts the Spectrum Eleven is a single instruction mode. As this is useful only during maintenance operations, this switch is normally left in the ON position.

Switches 2 - 5

These switches are used to select the data transmission rates for their respective lines and are set to suit the requirements of the terminals or other devices to be connected.

BAUD RATE	SW2	SW3	SW4	SW5
50	ON	ON	OFF	ON
75	ON	ON	OFF	OFF
110	OFF	OFF	OFF	OFF
134.5	ON	OFF	ON	ON
150	OFF	OFF	OFF	ON
200	ON	OFF	ON	OFF
300	OFF	OFF	ON	OFF
600	ON	OFF	OFF	ON
1200	OFF	ON	OFF	OFF
1800	OFF	ON	OFF	ON
2400	OFF	OFF	ON	ON
4800	OFF	ON	ON	OFF
9600	OFF	ON	ON	ON

Switch 6

This switch controls the conditional addition of a parity bit to each transmitted character. In the ON position, parity is enabled.

Switch 7

Normally, each character is terminated by one stop bit, achieved with switch 7 in the ON position. With switch 7 OFF, two stop bits are appended for character lengths of 6, 7 or 8 bits and 1.5 stop bits are appended to 5 bit characters.

Switches 8 and 9

These two switches control the character length (exclusive of parity, etc.) as follows:

SW8	SW9	CHAR LENGTH
OFF	OFF	8 bits
OFF	ON	7 bits
ON	OFF	6 bits
ON	ON	5 bits

Switch 10

This switch determines whether even or odd parity is to be generated. When switch 10 is OFF, even parity is selected.

6.2 'T' BOARD SWITCH SETTINGS

For 8-inch Drives

SW3	SW4	DISK TYPE
x	OFF	RK06 (8.5 Mb)
OFF	ON	RK07 (30 Mb)
ON	ON	RK07 (70 Mb)

x = Don't care

For 14-inch Drives

SW3	SW4	DISK TYPE
OFF	OFF	RK07 (2 x 28 Mb units)
OFF	ON	RK07 (4 x 33 Mb units)
ON	OFF	Native (1 x 56 Mb unit)
ON	ON	Native (1 x 132 Mb unit)

INTRODUCTION

This chapter specifies the backplane assignments for all Spectrum Eleven models. For a description of the interface boards designed and implemented by Webster Electronics, refer to the Engineering Section.

7.1 FEATURES

The Spectrum backplane assembly has the following features:

LSI-11 bus compatible.

4 quad slot capacity for desk-top cabinets and 6 quad slot capacity for rack-mount system cabinets. The backplane card frame will accept either double height or quad height modules, or an intermix of both.

All Q-bus data, control, and power connections are pre-wired on the printed circuit backplane to each module location.

A priority-structured I/O bus system based upon electrical position along the Q-bus. Device priority levels are established by a daisy-chained grant signal arrangement for interrupt and DMA requests. Placement of modules into the backplane automatically passes the bus grant signal to the next lower-priority device.

7.2 EXPANSION

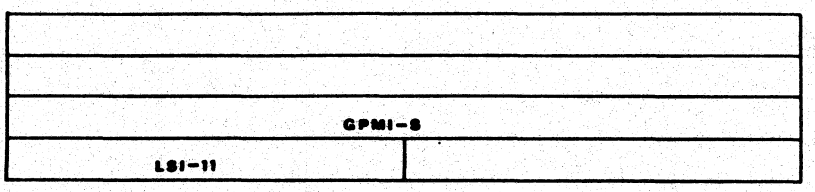
Refer to the diagrams on the following pages for the backplane assignments and expansion space available for each model.

7.3 PCBs NOT LINKED TO Q-BUS

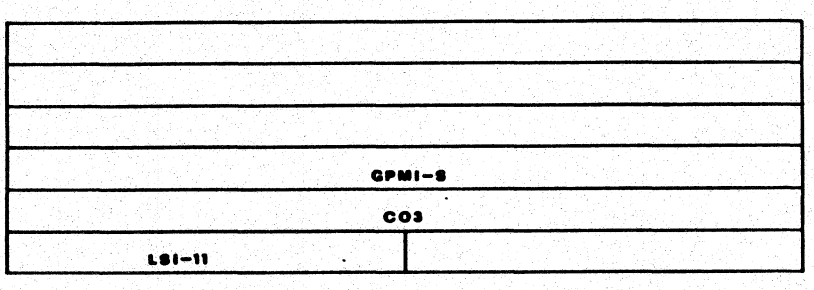
The B/M Board is attached to the GPMI-S by an internal bus.

7.4 BACKPLANE ASSIGNMENTS

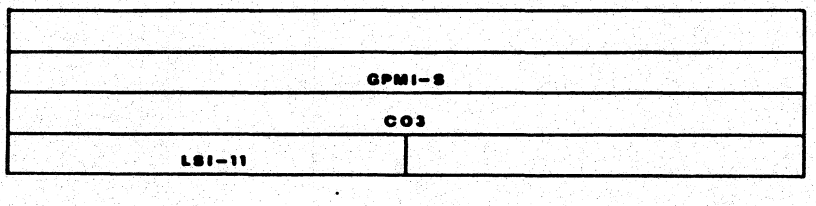
MODELS B & D



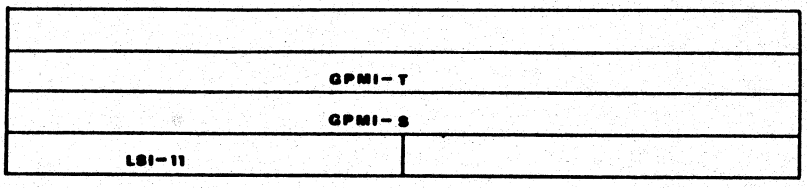
MODEL P



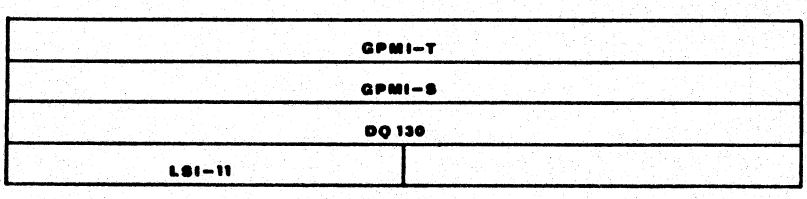
MODELS BP & DP



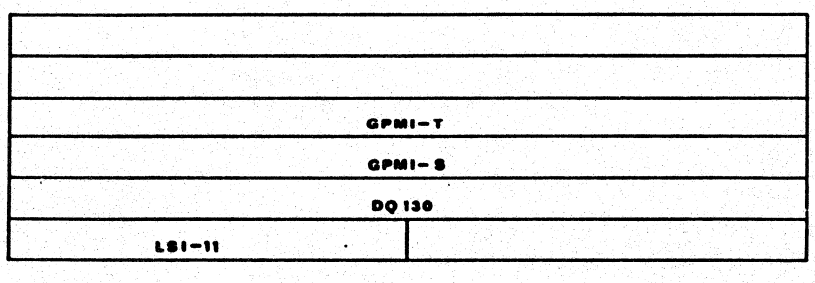
MODELS GC & HC



MODEL GCM



MODELS JM & KM



MODELS D5, D6

GPM1 - Y	
GPM1 - X	
LSI - 11/23	

MODELS GC5, GC6, HC5, HC6

GPM1 - T	
GPM1 - Y	
GPM1 - X	
LSI - 11/23	

MODELS JM7, KM7

GPM1-T	
GPM1-Y	
GPM1 - X	
GPM1 - X	
DQ130	
LSI - 11/23	

MODELS JM5, JM6, KM5, KM6

GPM1 - T	
GPM1 - Y	
GPM1 - X	
DQ130	
LSI - 11/23	

D A manual bootstrap can always be initiated by pressing the RESTART button.

E The CLOCK is activated when this button is depressed.

1.2 STARTUP PROCEDURES

1. Turn the power key clockwise.

2. If the floppy disks have been removed from the drives since the previous session, they are inserted after the power is on. Insert the SYSTEM disk face up (with the label on the top surface and nearest the drive opening) in Drive 0 (this being the left hand drive) and press the shutter door down. Insert the DATA disk (face up) in Drive 1 (the right hand drive) and press the shutter door down.

3. Press the RESTART button to load the operating system.

1.3 SHUTDOWN PROCEDURES

1. When the last job has been processed, control must be returned to the system monitor before any further steps are taken. This option is normally included with the application system.

2. It is not necessary to remove the SYSTEM or DATA disk before powering down the system. The disks may remain installed in the drives and only removed when required to run certain utilities. If the disks are to be removed, release the shutter doors of Drive 0 and Drive 1 and remove the disks.

3. Turn the power key anti-clockwise. It is not necessary to power off individual devices independently.

1.4 DATA BACKUP AND RECOVERY PROCEDURES

Whenever magnetic media are used with computer systems, it is considered essential that security copies of all important data files are maintained. The possibilities of corruption of data are always present; this being brought about by possible hardware failure, media failure, or accidental erasure through operator error. The cost of recovery can vary from near zero to infinity, depending on the availability of a recent backup copy. This becomes of paramount importance where large volumes of critical user data are being generated. With floppy disk systems where two drives are available,

INTRODUCTION

These instructions relate to a total floppy disk system, and to a floppy disk subsystem when configured with a cartridge disk system (refer Chapter 2) or a Winchester disk system (refer Chapter 3).

1.1 OPERATOR CONTROLS

These controls, located on the front panel of the machine, provide a fundamental link between the user and the computer, with full communication facilities being serviced through the console terminal.

The controls are either activating buttons or indicators (Figure 1-1).

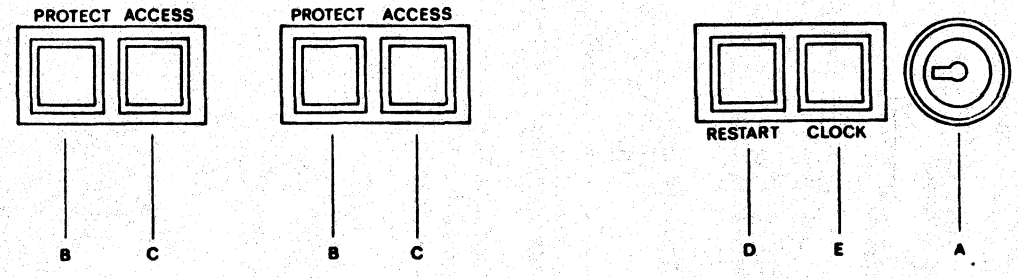


Figure 1-1

A The Spectrum Eleven power on/off control is activated by a key. When turned clockwise, power is ON and if the SYSTEM disk has been left in the machine during the previous power-down, bootstrap is initiated.

B PROTECT buttons can be depressed to protect the disk in that drive against an inadvertent write operation.

C ACCESS buttons are indicators which inform the user that the read/write head is loaded against the disk.

NB: On a Winchester disk drive, the ACCESS button can be depressed so that during bootstrap, the planned hierarchical sequence ignores the Winchester as the first option and bootstrap is initiated from the next bootable device. Refer Chapter 5 for details of bootstrap.

it is common practice to back up the disk or the important files on a regular basis, preferably at least once a session or day.

Two utilities are available for disk to disk copying on a total floppy system. They are FUTIL and BACKUP.

On a floppy disk sub-system configured with a cartridge disk system, files may be copied to floppy disk using the RT-11 COPY command.

On a floppy disk sub-system configured with a Winchester disk system, files are always backed up to floppy disks. Two utilities are available; either selected file copying or disk image copying to a series of floppy disks. The utilities are BAKFLP and SAVRES.

Instructions for using these utilities and the RT-11 command can be referenced in the Spectrum Eleven RT-11 Software Manual.

1.5 CARE OF FLOPPY DISKS

Like any other magnetic media floppy disks should be treated with care. To obtain the best performance and to provide the best protection for the data on the disk, the following should be adhered to.

1. The recording surface of the disk must not be touched.
2. The disk should be returned to it's protective envelope after use.
3. A felt-tipped pen should be used when writing on the label of the disk as pencils and ball point pens can make an impression on the surface of the disk, causing loss of data. An erasure should never be used as the small rubber particles can adhere to the recording surface.
4. Floppy disks should be stored in an upright position, preferably in the Supplier's box.
5. Floppy disks must be kept away from direct sunlight, magnetic fields, and extremes of temperature.
6. Floppy disks must not be folded or bent as correct contact will not be made with the read/write head.
7. Disks must not be loaded into the machine while power is off because disk motor rotation assists proper centering of the media. However it is permissible to leave media installed when powering off the system. Subsequent powering on will then initiate automatic bootstrap.

8. The floppy disk must be carefully but firmly loaded in the drive unit otherwise distortion may occur if it is not centered properly. This would cause the disk to rotate eccentricly and miss data.

1.6 LABELLING OF FLOPPY DISKS

The following points should be adhered to when labelling floppy disks.

1. The adhesive side of the label is not to touch the exposed magnetic disk surface.

2. The labels should be fixed at the top of the floppy disk as this will eliminate the risk of covering any of the holes and provide a guide for the operator when loading the disk.

3. As mentioned in the previous paragraph, use a felt-tipped pen to write on the label.

1.7 WRITE PROTECT FEATURE

Spectrum floppy disk drives and most floppy disks are equipped with a write protect feature. When using disks with this feature, ensure that the foil label provided by the manufacture has been applied over the write protect notch to allow writing. When the notch is exposed the drive will not write and any data on the disk is write protected. By removing the label after writing, this feature is very useful for securing archive copies of disks.

INTRODUCTION

These instructions relate to a total cartridge disk system. If the cartridge disk system is configured with a floppy disk sub-system, please refer to the preceding chapter for additional information.

2.1 OPERATOR CONTROLS

The operational controls and indicators (Figure 2-1) are located on the front panel of the disk drive. One or two rocker-type switches may be located behind the front panel to provide protection from inadvertent write operations, and control the illumination on the PROT indicators. All Spectrum machines are delivered with these rocker switches in the OFF position.

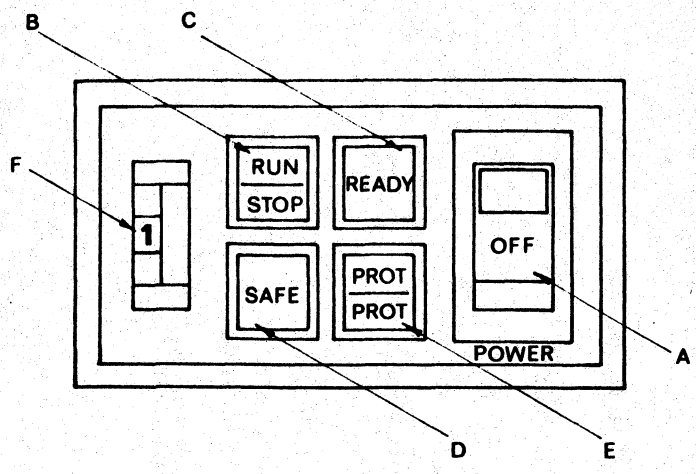


Figure 2-1

A The ON/OFF power control is a rocker-type switch/indicator. The indicator is illuminated when power is ON.

B The RUN/STOP control is a momentary action switch/indicator which provides a means for selecting the operational status of the drive. The control will be illuminated when actuated and the drive has been properly conditioned to allow the disk to be brought to operating speed.

When the illuminated switch/indicator is depressed again, a STOP sequence will be entered and the disk will decelerate to a stop. The cartridge may be unloaded at this time.

If a cartridge has been incorrectly inserted or an emergency condition exists, the operation of the RUN/STOP control is inhibited. Under this condition the control will not become illuminated and the Run status will not be achieved.

C READY is an indicator which is illuminated when the disk drive achieves a Ready condition. This is defined as follows:

All power is applied and correct
A cartridge is correctly inserted
The disk is rotating at the correct speed
The heads are loaded
No equipment faults are detected
The logic is prepared to recognize commands

D The SAFE indicator is illuminated when it is possible to safely insert or remove the disk cartridge. When the SAFE indicator is extinguished, protective cartridge locks prevent removal of the disk cartridge.

E The PROT (Protect) indicators which are mounted in a common housing, are provided to indicate the data protection status of the disks. These indicators illuminate when a write operation is inhibited.

F The unit number selection switch is always set to 1 for Spectrum machines.

2.2 STARTUP PROCEDURES

1. Turn power switch to ON and wait until the SAFE button illuminates. The door of the disk drive is locked until SAFE lights up. Ie., the disk can only be loaded/removed if this light is on.

2. Open the door of the drive carefully as it is subject to strong spring tension.

3. Place the 5Mb cartridge disk (face up) into the drive and push it firmly into place. Close the door.

4. Press the RUN/STOP button (the SAFE light extinguishes). This button illuminates and the disk will run up past running speed to promote a self-clean function.

5. When this operation is complete (approximately 2 minutes), the READY button will illuminate.

6. Press the RESTART button on the front panel of the Spectrum. This will commence the bootstrap procedure which is activated from RK0 (the name designated to the system disk).

2.3 SHUTDOWN PROCEDURES

1. When the last job has been processed, control must be returned to the system monitor before any further steps are taken. This option is normally included with the application system.

2. Press the RUN/STOP button. The READY and SAFE lights will go out and the disk commences to wind down. After approximatley 30 seconds, a distinct vibration can be heard as the cartridge stops. Wait for the SAFE button to illuminate before removing the disk cartridge.

3. Turn the Power key (on the Spectrum front panel) anti-clockwise. This puts the drive in a power off mode.

2.4 DATA BACKUP AND RECOVERY PROCEDURES

No special Webster support utility is available to backup or recover from a cartridge disk. This facility is normally provided with the application system software.

File copies are made using the RT-11 COPY command (refer Spectrum Eleven RT-11 Software Manual).

2.5 CARE OF CARTRIDGE DISKS

The following points should be noted for the care of cartridge disks:

1. The door of the drive should be kept closed when the cartridge is not inserted in the drive.

2. Cartridges should be stored either horizontally or vertically in their original containers or in any recommended storage, like zip-up plastic bags. Front load cartridges used in Spectrum machines should always be positioned to avoid objects which could damage the hub or cause the air inlet door to be pushed open.

3. Cartridge disks must not be stacked more than 5 high.

4. The cartridge must not be exposed to any magnetizing force in excess of 50 oersted or loss of data may result.

5. Cartridge disks must be kept away from direct sunlight.

2.6 LABELLING OF CARTRIDGE DISKS

1. Cartridge disks are to be labelled in the area of the label frame which is molded as part of the handle.

2. Placement of labels in any other areas may cause improper operation or contamination.

INTRODUCTION

These instructions relate to a Winchester disk system configured with a floppy disk sub-system or a magtape sub-system.

3.1 OPERATOR CONTROLS

The controls are either activating buttons or indicators.

Where 8-inch drives are configured the operator controls are identical to those found on a floppy disk system and with the exception of the ACCESS button, operate in the same manner.

On 14-inch drives (refer Figure 3-1), there is only one set of the Protect and Access buttons (**B** & **C**), and the Power key (**A**) is situated below the Magtape controls.

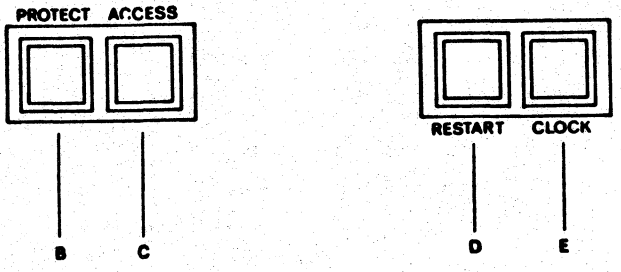


Figure 3-1

A The Spectrum Eleven power on/off control is activated by a key. When turned clockwise, power is ON and bootstrap is initiated.

B The (right-hand) PROTECT button can be depressed to protect the Winchester disk against an inadvertent write operation.

C The ACCESS button is an indicator to inform the user that a disk operation is taking place. It is also a switch to bypass the Winchester as the boot device. When ACCESS is depressed, the planned hierarchical sequence ignores the Winchester as the first option and bootstrap is initiated from the next bootable device.

D A manual bootstrap can always be started by depressing the RESTART button.

E The CLOCK is activated when this button is depressed.

3.2 STARTUP PROCEDURES

As the Winchester disk is a non-removable device, there is very little action to be taken.

1. Ensure that the ACCESS button is in the out position (assuming bootstrap is to be initiated from the Winchester disk).

2. Turn power key clockwise. The Winchester ACCESS button illuminates as the disk is powering up. After approximately 30 seconds, with the disk now running at the correct speed, automatic bootstrap is initiated. The RESTART button illuminates and the ACCESS indicator extinguishes.

3.3 SYSTEM SHUTDOWN PROCEDURES

1. When the last job has been processed, control should be returned to the system monitor before any further steps are taken. This option is normally included with the application system.

2. Turn the power key anti-clockwise. It is not necessary to power off individual devices independently.

3.4 DATA BACKUP AND RECOVERY PROCEDURES

As the Winchester is a non-removable device, it is extremely important that backup of files is done on a regular basis.

SAVRES is a utility that backs up the whole Winchester disk to a series of floppy disks or to a magnetic tape. If a selected file(s) is to be saved to floppy disk and the size of the file exceeds the size of a floppy disk (approximately 2432 available blocks) use the selected-file utility BAKFLP. Use the RT-11 COPY command to save small selected files to floppy disk or any selected file to magnetic tape.

Instructions for using these utilities and the RT-11 COPY command can be referenced in the Spectrum Eleven RT-11 Software Manual.

INTRODUCTION

The magnetic tape drive is housed in a rack with a Winchester disk system or a Winchester disk system configured with a floppy disk sub-system.

4.1 OPERATOR CONTROLS

The controls and indicators (Figure 4-1) are located on the front panel of the tape drive unit.

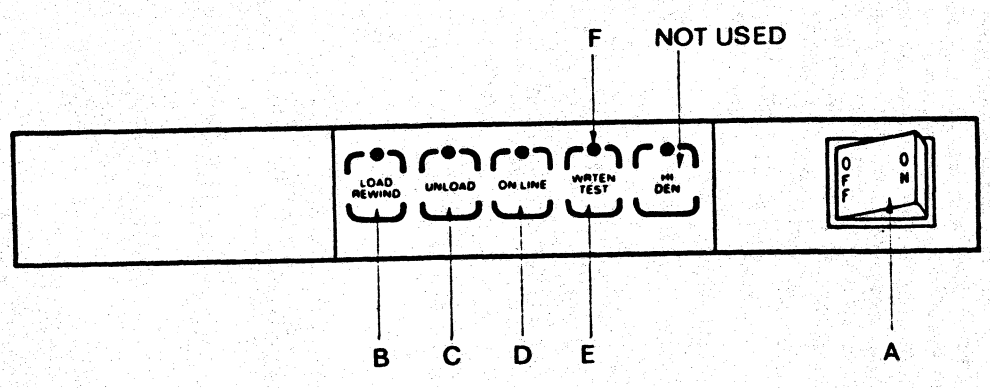


Figure 4-1

A Power is activated by an ON/OFF rocker switch and indicator.

B LOAD REWIND ia a tactile switch and indicator. Activating this switch loads tape to BOT marker. If the tape is positioned at a point other than the BOT marker and LOAD REWIND is pressed, it rewinds the tape to the BOT marker. The indicator is illuminated to indicate that the BOT tab is positioned at the photosensor. When this indicator is pulsing, the transport is executing a load or rewind sequence.

C UNLOAD is a tactile switch and indicator. When this is activated, it unloads the tape from any point. The indicator flashes during the unload sequence then remains illuminated. When the transport is in ON-LINE mode, the indicator is not illuminated.

D ON-LINE is a tactile switch and indicator which illuminates to indicate that the transport is on-line (sensed by BOT marker). A second depression switches the transport off-line and extinguishes the indicator.

E TEST is a tactile switch which selects alternate operational mode for the other switches. This switch is for maintenance testing purposes only.

F WRT EN (Write Enable) is an indicator only which illuminates to indicate a write function may be performed.

4.2 STARTUP PROCEDURES

1. Turn power switch ON and verify that UNLOAD is illuminated. Allow for normal delay of 2 seconds.
2. Ensure that tape is wound completely onto reel.
3. Open front-panel door by gently pressing down on top (centre) of door.
4. Insert tape (write-ring groove down) into front of unit and place over the hub.
5. Close door.
6. Activate LOAD switch. The access door is now locked. When the LOAD sequence is completed, the LOAD indicator remains illuminated.
7. Press ON-LINE switch.

NB: Both top cover (in a system configuration this is not exposed) and front panel door are locked during tape load functions. Any attempt to open either cover or door before tape is unloaded will result in mechanical damage to the locking mechanism.

4.3 SHUTDOWN PROCEDURES

1. Check that the transport is in off-line mode (ON-LINE indicator extinguished).
2. Activate UNLOAD switch. During the UNLOAD sequence, the UNLOAD indicator will pulse and the access door will remain locked. When the sequence is completed, UNLOAD indicator will remain illuminated and access door will unlock.
3. Open tape access door when the UNLOAD indicator remains illuminated without flickering.

4. Carefully remove tape reel by lifting the reel slightly up and then out towards you.

5. Close tape access door.

4.4 DATA REINSTATEMENT PROCEDURES

Data is saved onto magnetic tape via the utility SAVRES or by use of the RT-11 COPY command.

Note that selected files cannot be restored back to the Winchester from a SAVRES tape. Selected files may be restored only if they were saved with the RT-11 COPY command.

Refer to the Spectrum Eleven RT-11 Software Manual for details of SAVRES.

4.5 CARE OF TAPES

The following points should be noted for the care of magnetic tape.

1. The access door for the tape unit should always be kept closed except when loading or unloading a reel.

2. Special care should be taken when handling reels with apertures, to avoid damage to the edges of the tape. Nine-track tape is particularly sensitive to damage of this type.

3. The tape reels should be periodically inspected to ensure that they are not cracked or distorted.

4. The portion of tape between the BOT and EOT markers should never be touched and the free end of the tape should be kept clear of objects.

5. A contaminated reel of tape should not be used as this spreads dirt to clean tape reels and can affect tape drive operation.

6. Tape reels should be stored inside their containers which have been kept clean and closed while the reel is in use.

7. The tape drive is sensitive to dust, ash and paper particles generated from a line printer. Periodic cleaning will prevent frequent read and write errors.

8. The tape path should be cleaned regularly as part of preventive maintenance.

9. Tapes themselves should be periodically cleaned. This is dependent on the number of passes the tape has made and in accordance with the manufacturer's instructions.

4.6 LABELLING OF TAPES

1. Use sticky labels that can be easily removed and place the label on the hub of the reel away from the outside rim.

2. Always enter the date, time and file/job name.

INTRODUCTION

Bootstrap is a small program stored in non-volatile memory which is used to start the system. The bootstrapping process is entirely automatic and should always occur when the system is switched on. Bootstrap is initiated from first drive on line. Certain terminals however, if switched on at the same time as the Spectrum Eleven, will defeat the automatic power-on bootstrap unless the BREAK function is disabled (refer Section 2, paragraph 6.1). A re-boot may also be initiated without powering down by pressing the RESTART button. However, if RESTART is activated during processing, the program will abort.

5.1 SYSTEM STARTUP SEQUENCE

System startup is carried out in the following sequence:

Running the permanent bootstrap program (in ROM);

Loading and running the boot program on the first few blocks of disk;

Loading and running the RT-11 monitor itself;

RT-11 executing its startup command file.

5.2 BOOTSTRAP

The functions carried out when booting takes place are:

1. CPU and memory diagnostics are performed to ensure that the computer is functioning correctly. If a machine fails to 'boot' it means that the Bootstrap program has detected a fault.

2. The Bootstrap then checks the devices on the computer in sequence, and attempts to boot from the first ready device. The hierarchy is Winchester disk, floppy disks (from Drive 0 to the first drive containing a floppy disk), magnetic tape, and finally cartridge disk. If a device is on-line, an attempt is made to boot from it and with the exception of floppy disks, if multiple devices are present, a boot is only attempted from Unit zero.

3. The bootstrap program prints a message if an error is detected. These messages are:

?MEM	Memory test failure
?DM	Winchester disk failure
?SF	Hardware error while attempting to read floppy disk
?MT	Hardware error while attempting to read magnetic tape
?RK	Hardware error while attempting to read cartridge disk
?NO DEV	No boot device was on-line

4. If the bootstrap program functioned correctly, but the device that it tried to boot from did not have a bootable RT-11 system on it, the message 'No Boot on Disk' or 'No Boot on Volume' will appear and the program will stop. Check that the system disk is loaded (particularly if booting from a floppy disk) and/or check that the Boot program does exist on the System disk. Enter the command COPY/BOOT from the appropriate monitor being used, eg., RT11FB.SYS, to the device and re-boot. If successful, it signifys that the boot program was not previously on the disk.

5.3 CHECKOUT SEQUENCE

The bootstrap displays are in a form as illustrated in the following example:

RT-11SJ(S) V04.00

where -

RT-11	is the Operating system
SJ	stands for single job monitor. This may be replaced by the letters FB which designate a foreground-background monitor
(S)	stands for Sysgen (special generation of a system)
V04.00	is the version number of the Operating system. This example is version 4 with the next version number incrementing by one

This display is then followed by the commands used in the system startup command file and finally a monitor prompt represented by a dot. This prompt indicates that the system is in command mode and is expecting instructions from the operator via the console terminal. Refer to the RT-11 Operation Guide (Spectrum Eleven RT-11 Software Manual) for details of possible commands.

INTRODUCTION

If problems are experienced while operating the Spectrum Eleven, refer to this checklist before seeking further assistance.

If a negative response is applicable to the questions on the checklist, take corrective action as follows:

6.1 CHECKLIST

Are the fans running?

Check that the power supply is on.

Prove the power supply by trying other appliances.

Check that the key has been turned clockwise.

Inspect the fuses (which are integral with the power socket) and if they are faulty, remove the other devices from the Spectrum Eleven power outlets before replacing them with 5-amp fuses.

Does the RESTART indicator illuminate when power is applied?

Disconnect the serial lines and try again. If this procedure cures the problem, the BREAK disable switch may need to be turned on. Refer to Section 2, paragraph 6.1.

Does the RESTART indicator illuminate when the button is depressed?

The terminal may be off line (Local). Disconnect and try again.

When executing RESTART with no bootable device enabled, does a fault display appear on the console terminal?

The terminal may be faulty or wrongly connected in the output path. Test the terminal in local mode. Check that the line parameter switches are correctly set. Refer to Section 2, paragraph 6.1.

If the fault display is correct, do the Console ODT commands (Section 4, paragraph 1.2) work?

The terminal may be faulty or wrongly connected in the input path.

Does RT-11 load correctly from the System disk?

The System disk may be corrupted, damaged or overwritten. Attempt to load from an alternative bootable device.

Is the RT-11 TIME command working properly?

The CLOCK switch may be turned off.

Is there any peripheral device that is not working?

Check that all interconnecting leads are firmly plugged in and the ON switch of each peripheral is activated.

Where applicable, is the Winchester disk rotating?

Check that the ACCESS indicator is in the out position and press RESTART.

6.2 PROCEDURAL ERRORS

A common procedural error in non-Winchester systems is the removal of the System disk from its original drive while using the system commands. When it is necessary to remove the System disk, as is often required when using utility programs such as FUTIL or PIP, it should be arranged that the system drive be made WRITE PROTECT and used for read operations only. The System disk should then be replaced before using the 'Return to RT-11' option or CTRL/C to return to the keyboard monitor. The drive is then write-enabled. This procedure is the only safe way to protect data disks from inadvertent overwriting with system information.

1.1 USING CONSOLE ODT

In most SPECTRUM 11 applications, an interactive ASCII terminal is connected to serial port A. While the processor is in the HALT mode (the RESTART indicator light is extinguished), this terminal may be used to examine and deposit processor register and memory location contents and, to control the loading and execution of programs. The HALT mode may be entered by:

1. Executing the bootstrap while a system problem exists. For example, the System disk is not installed or enabled.
2. Pressing the BREAK key of the console terminal but only if this has been enabled (Refer to Section 2, paragraph 6.1 for details).
3. Under program control by executing an illegal instruction or a deliberate HALT instruction.

1.2 ODT COMMANDS

On entering the HALT mode, the processor outputs the 6-digit octal halt address to the terminal followed by either an '@' or a '\' character. At this point, any of the commands listed on the following page will be accepted -

COMMAND	EXAMPLE	FUNCTION
n/	1234/	Examine contents of memory location n
<LF>	<Line Feed Key>	Examine contents of location n+2
n/@	1234/(echo)@	Examine contents of location whose address is in location n
Rn/	R5/	Examine contents of CPU register n
RS/	RS/	Examine contents of processor status word
n/m<CR>	12/(echo)34<RET>	Deposit value m into memory location n
Rn/m<CR>	R5/(echo)67<RET>	Deposit value m into processor register n
P	P	Proceed or continue execution of program
nG	200G	Start program from location n
<DEL>	<DEL> or <RUB>	Delete last character entered
nL	177560L	Load program from paper tape reader at peripheral address n

This list details all salient assignments for the Spectrum Eleven.

Code

* - Extra memory accessible only by DMA devices and iterator or by SS23 models with memory management.

\# - Increments by 10 octal for each additional line.

$ - Address increments by 10 octal for each additional 8 lines. Vector increments by 4 octal for each additional 8 lines.

	Family	
ASSIGNMENT	SS11	SS23
Memory, 64Kb	000000-167776*	000000-177776
Memory, 128Kb	000000-167776*	000000-377776
Memory, 256Kb	000000-167776*	000000-767776*
Memory, 512Kb	000000-167776*	000000-767776*
Memory, 1Mb	000000-167776*	000000-767776*
Memory, 2Mb	000000-167776*	000000-767776*
Timeout, bus error trap	000004	000004
Illegal instruction trap	000010	000010
Break point trap, Trace trap	000014	000014
Input/output trap vector	000020	000020
Power fail vector	000024	000024
Emulator trap vector	000030	000030
Trap instruction vector	000034	000034
Serial line A receiver vector	000060	000060
Serial line A transmitter vector	000064	000064
Line time clock vector	000100	000100
Memory parity error trap	-	000114
Card Reader vector	000170	000170
Floppy disk vector	000174	000174
Line printer vector	000200	000200
Winchester disk vector	000210	000210
Magnetic tape vector	000224	000224
Iterator vector	000240	000240
KEV11/KEF11 float/point option vector	000244	000244
Memory Management	-	000250
Serial line B receiver vector	000270	000270
Serial line B transmitter vector	000274	000274
Additional Serial line vectors	000300#$	000300#$
SZV11 Multiplexer registers: CSR	160010$	760010$
RBUF	160012$	760012$
LPR	160012$	760012$
TCR	160014$	760014$
MSR	160016$	760016$
TDR	160016$	760016$

Magnetic Tape registers:	MTS	172520	772520
	MTC	172522	772522
	MTBRC	172524	772524
	MTCMA	172526	772526
	MTD	172530	772530
	MTRD	172532	772532
Bootstrap		173000-173774	773000-773774
Machine Version ID	MACH	173776	773776
Floppy Disk registers:	FDSEL	174200	774200
	FDCTRL	174202	774202
	FDMAR	174204	774204
	FDMXR	174256	774256
	FDTCR	174206	774206
	FDCSR	174210	774210
	FDTR	174212	774212
	FDSR	174214	774214
	FDDR	174216	774216
Card Reader registers:	CRCTRL	174220	774220
	CRMAR	174222	774222
	CRTCR	174224	774224
Iterator registers:	ITSAR	174240	774240
	ITSXR	174242	774242
	ITDAR	174244	774244
	ITDXR	174246	774246
	ITTCR	174250	774250
	ITFR	174252	774252
	ITCSR	174254	774254
Serial Line B regs:	RCSRB	175610	775610
	RBUFB	175612	775612
	XCSRB	175614	775614
	XBUFB	175616	775616
Additional Serial Line registers:		176500#	776500#
Cartridge registers:	RKDS	177400	777400
	RKER	177402	777402
	RKCS	177404	777404
	RKWC	177406	777406
	RKBA	177410	777410
	RKDA	177412	777412
	RKDB	177416	777416

Winchester registers:	RKCS1	177440	777440
	RKWC	177442	777442
	RKBA	177444	777444
	RKDA	177446	777446
	RKCS2	177450	777450
	RKDS	177452	777452
	RKER	177454	777454
	RKAS	177456	777456
	RKDC	177460	777460
->	RKBAX	177462	777462
	RKTYP	177466	777466

-> On parity memory systems only

Line Printer regs:	LPCTRL	177514	777514
	LPDATA	177516	777516
Serial Line A regs:	RCSRA	177560	777560
	RBUFA	177562	777562
	XCSRA	177564	777564
	XBUFA	177566	777566

The following is a brief listing of the Spectrum Eleven instruction set, intended for reference only. Explicit details can be referenced in the Microcomputer processor handbook which is available separately.

The SPECTRUM 11 and the SPECTRUM 23 relate to the LSI-11/02 processor and the LSI-11/23 processor respectively.

SINGLE OPERAND INSTRUCTIONS

SYMBOLIC	INSTRUCTION	OCTAL OP CODE
SWAB	swap destination bytes	0003DD
CLR(B)	clear destination	B050DD
COM(B)	complement destination	B051DD
INC(B)	increment destination	B052DD
DEC(B)	decrement destination	B053DD
NEG(B)	negate destination	B054DD
ADC(B)	add carry to destination	B055DD
SBC(B)	subtract carry	B056DD
TST(B)	test destination	B057DD
ROR(B)	rotate right	B060DD
ROL(B)	rotate left	B061DD
ASR(B)	arithmetic shift right	B062DD
ASL(B)	arithmetic shift left	B063DD
SXT	sign extend	0067DD
MTPS	move byte from source to processor status	1064SS
MFPS	move byte from processor status to destination	1067DD

BRANCH INSTRUCTIONS

BR	branch unconditionally	000400+BBB
BNE	branch if not equal (to zero)	001000+BBB
BEQ	branch if equal (to zero)	001400+BBB
BGE	branch if greater or equal (to zero)	002000+BBB
BLT	branch if less than (zero)	002400+BBB
BGT	branch if greater than (zero)	003000+BBB
BLE	branch if less than or equal (to zero)	003400+BBB
BPL	branch if plus	100000+BBB
BMI	branch if minus	100400+BBB
BHI	branch if higher	101000+BBB
BLOS	branch if lower or same	101400+BBB
BVC	branch if overflow is clear	102000+BBB
BVS	branch if overflow is set	102400+BBB
BCC	branch if carry is clear	103000+BBB
BHIS	branch if higher or same	103000+BBB
BCS	branch if carry is set	103400+BBB
BLO	branch if lower	103400+BBB

DOUBLE OPERAND INSTRUCTIONS

MOV(B)	move source to destination	B1SSDD
CMP(B)	compare source with destination	B2SSDD
BIT(B)	bit test source with destination	B3SSDD
BIC(B)	bit clear source to destination	B4SSDD
BIS(B)	bit set source to destination	B5SSDD
ADD	add source to destination	06SSDD
SUB	subtract source from destination	16SSDD
XOR	exclusive or source to destination	074RDD

MISCELLANEOUS INSTRUCTIONS

HALT	halt	000000
WAIT	wait for interrupt	000001
RTI	return from interrupt	000002
BPT	breakpoint trap	000003
IOT	input/output trap	000004
RESET	reset all bus devices	000005
RTT	return from interrupt	000006
JMP	jump unconditionally	0001DD
RTS	return from subroutine	00020R
NOP	no operation	000240
CLC	clear C bit of processor status	000241
CLV	clear V	000242
CLZ	clear Z	000244
CLN	clear N	000250
CCC	clear all condition codes	000257
SEC	set C	000261
SEV	set V	000262
SEZ	set Z	000264
SEN	set N	000270
SCC	set all condition codes	000277
JSR	jump to subroutine	004RDD
MARK	special subroutine return	0064NN
SOB	decr reg. and branch back if non zero	077RNN
EMT	emulator trap	104000-104377
TRAP	user trap	104400-104777

EXTENDED INSTRUCTIONS (KEV11 OPTION ONLY)

MUL*	multiply register contents by source	070RSS
DIV*	divide register contents by source	071RSS
ASH*	arithmetic shift register NN places	072RNN
ASHC*	arithmetic shift register pair NN places	073RNN
FADD	floating add (operands on register stack)	07500R
FSUB	floating subtract	07501R
FMUL	floating multiply	07502R
FDIV	floating divide	07503R

* standard for the SPECTRUM 23 only.

EXTENDED INSTRUCTIONS (KEF11 OPTION ONLY)

CFCC	copy floating condition codes	170000
SETF	set floating mode	170001
SETI	set integer mode	170002
SETD	Set floating double mode	170011
SETL	set long integer mode	170012
LDFPS	load FPP program status	1701SS
STFPS	store KEF11-AA's program status	1702DD
STST	store KEF11-AA's status	1703DD
CLRF,CLRD	clear floating/double	1704DD
TSTF,TSTD	test floating/double	1705DD
ABSF,ABSD	make absolute floating/double	1706DD
NEGF,NEGD	negate floating /double	1707DD
MULF,MULD	multiply floating/double	171RSS
MODF,MODD	multiply & separate integer and fraction floating/double	171(R+4)SS
ADDF,ADDD	add floating/double	172RSS
LDF,LDD	load floating/double	172(R+4)SS
SUBF,SUBD	subtract floating/double	173RSS
CMPF,CMPD	compare floating/double with accumulator	173(R+4)SS
STF,STD	store floating/double	174RDD
DIVF,DIVD	divide floating/double	174(R+4)SS
STEXP	store exponent	175RDD
STCFI,STCFL) STCDI,STCDL)	store and convert from floating or double) to integer or long integer)	175(R+4)DD
STCFD,STCDF	store and convert from floating to double and from double to floating	176RDD
LDEXP	load exponent	176(R+4)SS
LDCIF,LDCID) LDCLF,LDCLD)	load and convert integer or long integer) to floating or double precision)	177RSS
LDCDF,LDCFD	load and convert from double to floating and from floating to double	177(R+4)SS

Legend for OpCode Symbols

B	0 for word operations, 1 for byte operations
SS	source operand descriptor, 6 bits
DD	destination operand descriptor, 6 bits
R	register descriptor, 3 bits
BBB	branch offset argument, 8 bits representing -128 to +127 words
NN	6 bit numeric argument

Source (SS) and Destination (DD) Operand Descriptors

Symbol	Addressing Mode	Interpretation	Value
R	register	R is operand	00-07
(R)	register deferred	R is address	10-16
(R)+	auto increment	R is address, then incremented	20-26
#n	immediate	operand follows instruction	27
@(R)+	auto incr deferred	R is adrs of adrs, then incr	30-36
@#A	absolute	adrs of opr follows instr	37
-(R)	auto decrement	R is decremented, then adrs	40-46
@-(R)	auto decr deferred	R is decr, then adrs of adrs	50-56
X(R)	indexed	R + offset following instr is adrs	60-66
A	relative	R7 + offset following instr is adrs	67
@X(R)	index deferred	R + offs foll instr is adrs of adrs	70-76
@A	relative deferred	R7 + offs foll instr is adrs of adrs	77

Processor Status Byte (CPU internal control register)

SPECTRUM 11

Bit	00	C	Carry flag	Previous operation resulted in arith carry
Bit	01	V	Overflow flag	Previous operation resulted in arith overflow
Bit	02	Z	Zero flag	Result of previous operation was zero
Bit	03	N	Negative flag	Result of previous operation was negative
Bit	04	T	Trace bit	Force trap to 14 after each instruction
Bit	07		Priority bit	Inhibits interrupts

SPECTRUM 23

Bit 00	C	Carry flag	Previous operation resulted in arith carry
Bit 01	V	Overflow flag	Previous operation resulted in arith overflow
Bit 02	Z	Zero flag	Result of previous operation was zero
Bit 03	N	Negative flag	Result of previous operation was negative
Bit 04	T	Trace bit	Force trap to 14 after each instruction
Bits 05-07		Priority bit	Inhibit interrupts
Bits 08-11		Unused	
Bits 12,13	PM	Previous mode	Used with memory management to indicate what was last MMU mode
Bits 14,15	CM	Current mode	Indicate the present memory management mode

INTRODUCTION

Three DEC serial line interface options and the two standard SPECTRUM serial line connections will be discussed in this chapter. The programming of all these devices is identical in most respects, as discussed in paragraph 4.3 .

In addition, the SZV11 asynchronous multiplexer is described separately in the next chapter.

4.1 STANDARD SERIAL LINES

Two serial line connections are a standard part of the General Purpose Multiple Interface (GPMI Controller), where Serial Line A has been designated as the console device and Serial Line B as the second module. The address and vector settings of these two lines are 177560/060 and 175610/270 respectively. These lines have independent switch settable line parameters and baud rates 50 to 9600 baud. Additional controls include reader run, output break, and an EIA status input.

4.2 ADDITIONAL SERIAL LINES

When configured on a SPECTRUM 11, the start address of each additional line on the controller will increment by 10 octal from a starting address of 176500 and the interrupt vectors by 10 octal from a starting address of 300.

DLV11-E (Identification M8017)

The DLV11-E is a single asynchronous line interface module which offers full modem control and EIA-type interface. This module features program settable baud rates 50 to 19,200, but omits the reader run logic.

DLV11-F (Identification M8028)

The DLV11-F also features program settable baud rates 50 to 19,200, but omits some modem controls. Extra features of this interface are 20 mA current loop support and reader run control.

DLV11-J (Identification M8043)

The DLV11-J is a 4-channel asynchronous serial line unit that transmits and receives data from the peripheral device over EIA "data leads only" lines which do not use control lines. Each line has jumper-selectable baud rates 150 to 38,400, and optional extra support of 20 mA current loop and reader run control.

4.3 DEVICE REGISTERS

Four registers are available for use by each of these serial line interfaces. They have been defined as -

Receiver Control and Status register (RCSR)
Receiver Data Buffer Register (RBUF)
Transmitter Control and Status Register (XCSR)
Transmitter Data Buffer Register (XBUF)

Control and Status Registers

These two registers contain ready status and interrupt control bits associated with their respective data buffers.

Data Buffers

These buffers provide double-buffering in that one byte of data can be held while another byte is entering or exiting. This allows asynchronous, full duplex operation. Data is handled in the low byte of the registers. The buffer control circuitry places receiver buffer error flag bits in the high byte of the RBUF.

The bits in each register may vary slightly with each interface and these differences/exceptions are highlighted in the register descriptions that follow:

RECEIVER CONTROL AND STATUS REGISTER (RCSR)

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
GPMI	DSS	0	0	0	0	0	0	0	DONE	IE	0	0	0	0	0	RE
-E	DSI	RS	CLE	CAR	RA	REC	0	0	DONE	IE	DIE	0	SEND	REQ	RDY	0
-F	0	0	0	0	REC	0	0	0	DONE	IE	0	0	0	0	0	RE
-J	0	0	0	0	0	0	0	0	DONE	IE	0	0	0	0	0	RE

Figure 4-1 Control and Status Register (RCSR)

This is a Read/Write register.

RCSR<00> - Reader Enable (RE)

This bit is not applicable for DLV11-E.

This reader enable bit is set by program control to advance the paper tape reader or similar device to input a new character. Automatically cleared by the new character's start bit.

RCSR<01-05>

These bits are used by the DLV11-E only. For other interfaces they are read as zero.

RCSR<01> - Data Terminal Ready (RDY)

This is a control output lead to the data set communication channel. When set, permits connection to the channel. When reset, logically disconnects the interface from the channel. Must be cleared by program; not cleared by INIT.

RCSR<02> - Request to Send (REQ)

A control lead to the data set which is required for transmission. Cleared by INIT.

RCSR<03> - Secondary/Supervisory Transmitted Data (SEND)

This bit provides a transmit capability for a reverse channel of a remote station. When set, transmits a space. Cleared by INIT.

RCSR<05> - Data Set Interrupt Enable (DIE)

When set, allows an interrupt sequence to start when Bit 15 sets. Cleared by INIT.

RCSR<06> - Receiver Interrupt Enable (IE)

Set under program control to generate a receiver interrupt request when a character is ready for input to the processor (Bit 7 is set). Cleared under program control or by the BINIT signal.

RCSR<07> - Receiver Done (DONE)

Set when an entire character has been received and is ready for input to the processor. This bit is automatically cleared when RBUF (RXDATA) is addressed, when BINIT L or BDCOK H signal goes low or when reader enable bit is set. If Bit 06 is set, the setting of this Bit 7 starts an interrupt sequence.

RCSR<10> - Secondary/Supervisory Received Data (REC)

Applicable to DLV11-E only.

This status input bit provides a receive capablility for the reverse channel of a remote station. A space is read as a 1.

RCSR<11> - Receiver Active (RA)

Applicable to DLV11-E/F only.

When set, this bit indicates that the interface receiver is active. The bit is set at the centre of the start bit, which is the beginning of the input serial data from the device and is cleared by the leading edge of RCSR07 or INIT.

RCSR<12> - Carrier Detect (CAR)

Applicable to DLV11-E only; other interfaces not used and read as zero.

This bit is set when the data carrier is received. When reset, it indicates either the end of the current transmission or an error condition.

RCSR<13> - Clear to Send (CLE)

Applicable to DLV11-E only; other interfaces not used and read as zero.

The state of this bit is dependant on the state of the clear to send signal from the data set. When set, this bit indicates an ON condition; when reset, it indicates an OFF condition.

RCSR<14> - Ringing Signal (RS)

Applicable to DLV11-E only; other interfaces not used and read as zero.

When set, indicates that a ringing signal is being received from the data set. The ringing signal is not a level but an EIA control with a duty cycle of 2 seconds ON and 4 seconds OFF.

RCSR<15> - Data Set Interrupt (DSI)

Applicable to GPMI and DLV11-E only.

In the DLV11-E, this bit initiates an interrupt sequence provided RCSR05 is also set. This bit is set whenever RCSR 10, 12 or 13 change state. Is also set when RCSR14 changes from 0 to 1. Cleared by INIT or by reading the RCSR. Because reading the register clears the bit, it is in effect a 'read-once' bit.

In the GPMI, this bit simply reflects the state of the EIA status input line, and does not generate interrupts.

RECEIVER DATA BUFFER REGISTER (RBUF)

	15														00
-E/F/J	ERR	OER	FE	PE	0	0	0	0	DAT	DAT	DAT	DAT	DAT	DAT	DAT	DAT
GPMI	0	0	0	0	0	0	0	0	DAT	DAT	DAT	DAT	DAT	DAT	DAT	DAT

Figure 4-2 Receiver Data Buffer Register (RBUF)

This is a Read Only Register.

RBUF<00-07> - Received Data (DAT00-07)

These bits hold the character just read. If less than eight bits are selected, then the buffer is right-justified into the least significant bit positions. In this case, the higher or unused bits are read as zeros. Not cleared by INIT.

RBUF<12> - Parity Error (PE)

Not used by GPMI, read as zero.

When set, indicates that parity received does not agree with the expected parity. This bit is always 0 if no-parity operation is configured for the channel. Error bits remain valid until the next character is received, at which time the error bits are updated. Cleared by INIT.

RBUF<13> - Framing Error (FE)

Not used by GPMI, read as zero.

When set indicates that the character read had no valid stop bit. Cleared by BINIT signal.

RBUF<14> - Overrun Error (OER)

Not used by GPMI, read as zero.

When set, indicates that the reading of the previously received character was not complemented (receiver done not cleared) prior to receiving a new character. Cleared by BINIT signal.

RBUF<15> - Error Condition (ERR)

Not used by GPMI, read as zero.

Used to indicate that an error condition is present. This bit is the logical OR of RBUF 14, 13 and 12. Whenever one of these bits is set it causes RBUF15 to set. This bit is not connected to the interrupt logic. Error indications remain present until the next character is received, at which time the error bits are updated. INIT clears error bits.

TRANSMIT CONTROL AND STATUS REGISTER (XCSR)

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
-E/F	BRS	BRS	BRS	BRS	BRE	0	0	0	TR	TIE	0	0	0	MF	0	BRK
-J	0	0	0	0	0	0	0	0	TR	TIE	0	0	0	0	0	BRK
GPMI	0	0	0	0	0	0	0	0	TR	TIE	0	0	0	0	0	BRK

Figure 4-3 Transmit Control & Status Register (XCSR)

This is a Read/Write Register.

XCSR<00> - Break (BRK)

When this Break bit is set, it transmits a continuous space to the external device. Cleared by INIT. When not set, normal character transmission can occur.

XCSR<02> - Maintenance Function (MF)

Not used by GPMI or DLV11-J, read as zero.

When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receive serial input. It also forces the receiver to run at transmitter baud rate speed when common speed operation is enabled.

XCSR<06> - Transmitter Interrupt Enable (TIE)

When set, this transmitter interrupt enable bit allows an interrupt sequence to start when bit 7 is set. Cleared by program control or the BINIT signal.

XCSR<07> - Transmitter Ready (TR)

This bit is set when the transmitter buffer can accept another character. When set it initiates an interrupt sequence provided XCSR06 is also set. Automatically cleared when XBUF is loaded.

XCSR<11> - Programmable Baud Rate Enable (BRE)

Not used by GPMI or DLV11-J, read as zero.

This bit must be set to select a new baud rate indicated by XCSR 12-15.

XCSR<12-15> - Programmable Baud Rate Select (BRS)

Not used by GPMI or DLV11-J, read as zeros.

When set, these bits choose a baud rate from 50-19,200 as shown in the following table:

TABLE 4-1 BAUD RATE SELECTION

Program Control Receive jumpers Transmit Jumpers	Bit 15 R3 T3	Bit 14 R2 T2	Bit 13 R1 T1	Bit 12 R0 T0	Bit 11* Baud Rate
	I	I	I	I	50
	I	I	I	R	75
	I	I	R	I	110**
	I	I	R	R	134.5
	I	R	I	I	150
	I	R	I	R	300
	I	R	R	I	600
	I	R	R	R	1200
	R	I	I	I	1800
	R	I	I	R	2000
	R	I	R	I	2400
	R	I	R	R	3600
	R	R	I	I	4800
	R	R	I	R	7200
	R	R	R	I	9600
	R	R	R	R	19200

I = Jumper inserted = program bit cleared
R = Jumper removed = program bit set

* Bit 11 of the XCSR (write-only bit) must be set in order to select a new baud rate under program control. Also jumper PB must be inserted to enable baud rate selection under program control.

** When configured for 110 baud, the UART is set for two stop bits.

TRANSMIT DATA BUFFER REGISTER (XBUF)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	DAT	DAT	DAT	DAT	DAT	DAT	DAT	DAT

Figure 4-4 Transmit Data Buffer Register (XBUF)

This is a Write only register.

XBUF<00-07> - Data (DAT00-07)

Holds the character to be transferred to the external device. If fewer than eight bits are used, the characters must be loaded right-justified to the least significant bits.

INTRODUCTION

The SZV11 is an asynchronous multiplexer interface module that inter-connects the Q-bus with up to eight asynchronous serial data communications channels. It offers full modem control and EIA type interface. The SZV11 also features selectable baud rates of 50 to 19,200, and configuration for different serial data format parameters which includes character length, number of stop bits, and parity.

This chapter discusses the SZV11's internal registers and the function of each bit.

5.1 DEVICE REGISTERS

There are six addressable registers in the SZV11 which are addressed by only four addresses. These registers have been defined as:

Control and Status Register (CSR)
Receiver Buffer Register (RBUF)
Line Parameter Register (LPR)
Transmit Control Register (TCR)
Modem Status Register (MSR)
Transmit Data Register (TDR)

Registers RBUF and LPR, and MSR and TDR, are differentiated using Read Only and Write Only instructions. Consequently, DATIP (read-modify-write) instructions may not be used with addresses 76xxx2 and 76xxx6.

CONTROL AND STATUS REGISTER - (CSR)

The CSR register (Figure 5-1) contains the status of flags and control bits for line scanning, interrupts, and clearing. Write-only and not-used bits are read as zeros. Read-only bits are not affected by attempts to write into them.

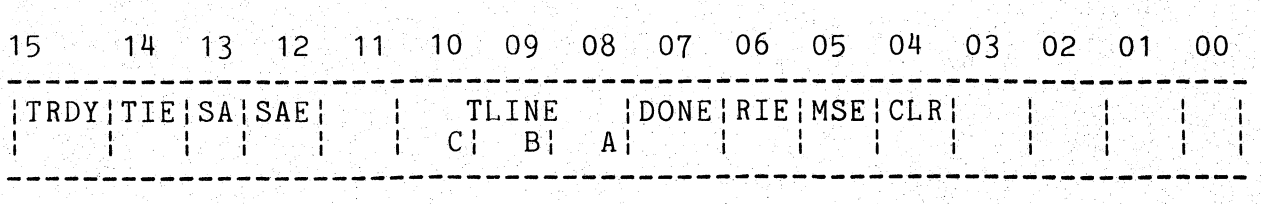


Figure 5-1 Control and Status Register (CSR)

CSR<04> - Clear (CLR)

When set, clears the receiver silo, all UARTs, and the Control and Status Register. Following CLR, the CSR and line parameters must be loaded again.

CSR<05> - Master Scan Enable (MSE)

Enables scanning of receivers, transmitters, and silo. Cleared by CLR or INIT.

CSR<06> - Receiver Interrupt Enable (RIE)

Enables receiver interrupt. Cleared by CLR or INIT.

CSR<07> - Receiver Done (DONE)

DONE is set by hardware, generating a receive interrupt if RIE is set, and SAE is cleared. DONE is cleared when the RBUF is read and is set again when the next word reaches the RBUF. If RIE is cleared, DONE may be used to indicate that the silo contains a character. If SAE is set, DONE has the same effect but does not generate interrupts.

CSR<08-10> - Transmit Line (TLINE)

If TRDY is set, TLINE A, B, and C indicate the number of the line which is ready to transmit a character. TRDY is cleared when the character is loaded into the transmit buffer, but is set again if another line is ready to transmit. These bits return to select line 0 following CLR or INIT. The line numbers are read as follows:

BIT	10	09	08	=	LINE
	0	0	0	=	1
	0	0	1	=	2
	0	1	0	=	3
	0	1	1	=	4
	1	0	0	=	5
	1	0	1	=	6
	1	1	0	=	7
	1	1	1	=	8

CSR<12> - Silo Alarm Enable (SAE)

SAE enables the silo alarm, preventing DONE from generating interrupts. When RIE is set, SAE allows SA to cause an interrupt after 16 entries to the silo. If RIE is cleared, SA may be used as a flag. Cleared by CLR or INIT.

CSR<13> - Silo Alarm (SA)

SA is set by hardware when 16 characters have been entered into the silo. If RIE is set SA causes an interrupt. SA is cleared when the RBUF is read, and is cleared by either CLR or INIT. When SA is set, the silo must be emptied because SA will not be set again until 16 characters have again entered the silo.

CSR<14> - Transmit Interrupt Enable (TIE)

TIE allows an interrupt to be set if TRDY is set.

CSR<15> - Transmitter Ready (TRDY)

TRDY is set by hardware when the scanner finds a line with its transmit buffer empty, and with its line enable bit set. TRDY is cleared when the TBUF register is loaded, and is cleared by CLR or INIT.

RECEIVER BUFFER REGISTER - (RBUF)

The Receiver Buffer Register (Figure 5-2) contains the received character bits, along with line number, error status, and valid data flags. RBUFis accessed by a read-only operation, using only word (not byte) instructions. A character will be lost if either the TST or BIT instruction is used. MSE bit 05 in CSR must be set for RBUF to operate.

Each time RBUF is read, characters are advanced through the silo and the next character becomes available to the program. A CLR or INIT operation empties the silo and causes RBUF bits 00-14 to become invalid. DV is cleared to zero by either CLR or INIT.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DV	OVRN	FE	PE			RLINE		RB	RB	RB	RB	RB	RB	RB	RB
					C	B	A	D7	D6	D5	D4	D3	D2	D1	D0

Figure 5-2 Receiver Buffer Register (RBUF)

RBUF<00-07> - Received Character (RB)

The received character RB read from the bottom of the silo. If the character length is less than eight bits, the higher-order bits are forced to zero.

RBUF<08-10> - Line Number (RLINE)

Encoded number of the line (1-8) through which the character was received. The line numbers are read as follows:

BIT 10	09	08	=	LINE
0	0	0	=	1
0	0	1	=	2
0	1	0	=	3
0	1	1	=	4
1	0	0	=	5
1	0	1	=	6
1	1	0	=	7
1	1	1	=	8

RBUF<12> - Parity Error (PE)

Bit set if received character had a parity error. Parity error bit is generated by hardware and does not appear in the RB data character.

RBUF<13> - Framing Error (FE)

Bit set if Stop bit did not appear in the predicted position as the character was received. This bit may be used for Break detection.

RBUF<14> - Overrun Error (OVRN)

Bit set if a character is received by a full silo before the current RB is read, causing receiver buffer to overflow. A character is lost but the received character put in the silo is valid.

RBUF<15> - Data Valid (DV)

Bit set if character read from RB is valid. An empty silo (invalid character) is indicated when DV bit 15 is cleared. Cleared by CLR or INIT.

LINE PARAMETER REGISTER - (LPR)

The 16-bit write-only LPR (Figure 5-3) contains the programmed line parameters for each line. Bits 00-02 select the line for parameter loading. Parameters must be reloaded following CLR bit 04 in CSR or INIT. Note that BIS or BIC instructions, or byte operations, are not allowed.

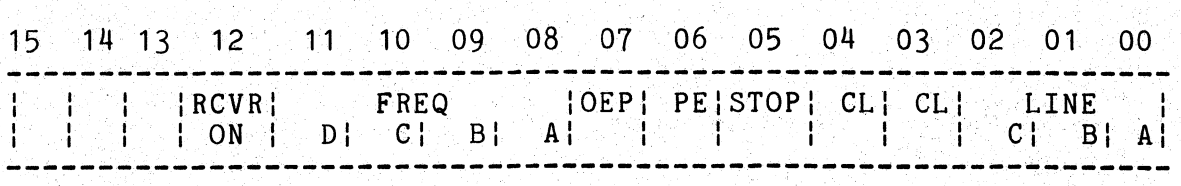


Figure 5-3 Line Parameter Register (LPR)

LPR<00-02> - Line Number (LINE)

Encodes the number of the serial line for which parameter information is to be loaded. The line numbers are read as follows:

BIT 02	01	00	=	LINE
0	0	0	=	1
0	0	1	=	2
0	1	0	=	3
0	1	1	=	4
1	0	0	=	5
1	0	1	=	6
1	1	0	=	7
1	1	1	=	8

LPR<03-04> - Character Length (CL)

Number of bits in the data character (not including parity bit). The character bits are as follows:

BIT 04	03	=	CHAR.BITS
0	0	=	5
0	1	=	6
1	0	=	7
1	1	=	8

LPR<05> - Stop Code (STOP)

Sets number of stop bits. 'Zero' = one-unit stop. 'One' = two-unit stop, or 1.5-unit stop for a 5-bit character length.

LPR<06> - Parity Enable (PE)

If set, parity is enabled for both transmit and receive. If not set, parity is disabled.

LPR<07> - Parity (OEP)

Set = odd parity. Not set = even parity. PE must be set to enable parity.

LPR<08-11> - Baud Rate Select (FREQ)

Select transmit and receive baud rates for selected line. The baud rates for the bits are as follows:

BIT 11	10	09	08	=	RATE	
0	0	0	0	=	50	*
0	0	0	1	=	75	
0	0	1	0	=	110	
0	0	1	1	=	134.5	
0	1	0	0	=	150	
0	1	0	1	=	300	
0	1	1	0	=	600	
0	1	1	1	=	1,200	
1	0	0	0	=	1,800	
1	0	0	1	=	2,000	
1	0	1	0	=	2,400	
1	0	1	1	=	3,600	*
1	1	0	0	=	4,800	
1	1	0	1	=	7,200	*
1	1	1	0	=	9,600	
1	1	1	1	=	19,200	

Note:

Machines currently installed with an eight channel asynchronous multiplexer use baud rates as shown in the above table. Baud rates denoted by an asterisk (*) will change as follows for all machines acquired as from January 1983.

50 becomes 75
3,600 becomes 4,800
7,200 becomes 9,600

LPR<12> - Receiver On (RCVR ON)

If set, enables receiver. Bit is turned off by either CLR or INIT. (Note that the transmitter clock is always on).

TRANSMIT CONTROL REGISTER - (TCR)

15							00								
DTR 7	DTR 6	DTR 5	DTR 4	DTR 3	DTR 2	DTR 1	DTR 0	LE 7	LE 6	LE 5	LE 4	LE 3	LE 2	LE 1	LE 0

Figure 5-4 Transmit Control Register (TCR)

The Transmit Control Register (Figure 5-4) contains two bytes. The low-byte contains eight bits selecting one of eight lines. The line is selected to transmit when the related bit is set. The low byte is cleared by either CLR or INIT. The high byte contains Data Terminal Ready bits, one for each line. Cleared only by INIT.

MODEM STATUS REGISTER - (MSR)

15							00								
CO 7	CO 6	CO 5	CO 4	CO 3	CO 2	CO 1	CO 0	RI 7	RI 6	RI 5	RI 4	RI 3	RI 2	RI 1	RI 0

Figure 5-5 Modem Status Register - (MSR)

The read-only Modem Status Register (Figure 5-5) contains two bytes. The low byte monitors and contains the status of each line's Ring Indicator (RI) lead. The high byte monitors and contains the status of each line's Carrier (CO) lead.

The MSR is not cleared by either CLR or INIT.

TRANSMIT DATA REGISTER - (TDR)

15							00								
BRK 7	BRK 6	BRK 5	BRK 4	BRK 3	BRK 2	BRK 1	BRK 0	TB 7	TB 6	TB 5	TB 4	TB 3	TB 2	TB 1	TB 0

Figure 5-6 Transmit Data Register (TDR)

The Transmit Data Register (Figure 5-6) contains two bytes. The low byte is the transmitter buffer register (TB) and contains the character to be transmitted. The high byte contains a Break bit for each line. When a Break bit is set, the related line begins sending zeros continually until the bit is cleared. The entire register is cleared by either CLR or INIT.

BIS or BIC instructions cannot be used. A character loaded into the TB must be right-justified if it has fewer than eight bits.

INTRODUCTION

In the GPMI-S there are two registers which interface to the line printer. Where an additional line printer is present, an EIA serial line controller is configured. Refer to 'Serial Line Programming Guide' for information on these registers.

6.1 DEVICE REGISTERS

Within the control unit there are two registers, one for the printer status, the other to hold the 7-bit ASCII-coded character to be printed. The same register addresses and bit definitions are used.

LINE PRINTER CONTROL AND STATUS REGISTER (LPCTRL)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	0	0	0	0	0	0	0	DONE	IE	0	0	0	0	0	0

Figure 6-1 Control and Status Register (LPCTRL)

This is a Read/Write register with bits 7 and 15 Read only.

LPCTRL<06> - Interrupt Enable (IE)

This interrupt enable bit is set to allow Done to cause an interrupt.

LPCTRL<07> - Data Request (DONE)

The read only bit Done is set whenever printer is ready for next character to be loaded. Indicates that previous function is either complete or has been started and continued to a point when the printer may accept the next command. Set only by printer condition. Will not be set if printer is Off-Line.

LPCTRL<15> - Printer Not Ready (ERR)

This bit is set when an error condition exists in the printer, ie., no stationery, power off, printer placed Off-Line, etc. Bit is reset only by manual correction of error condition.

LINE PRINTER DATA BUFFER REGISTER (LPDATA)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	DAT	DAT	DAT	DAT	DAT	DAT	DAT

Figure 6-2 Data Buffer Register (LPDATA)

This register is Write only.

LPDATA<00-06> - Transmit Data (DAT00-06)

ASCII-coded data for the character to be printed.

INTRODUCTION

The Spectrum Eleven contains, within the GPMI-S, an "Iterator". This device is capable of performing direct memory array operations independently of and concurrently with the LSI-11 CPU, and generating interrupt on completion. Operations currently defined are:

performing block memory moves;
setting up blocks of memory to any value;
performing "Well" type memory tests.

The last two functions are used by the bootstrap to initialize and test memory.

8.1 DEVICE REGISTERS

SOURCE MEMORY ADDRESS REGISTER (ITSAR)

15															00
SA 15	SA 14	SA 13	SA 12	SA 11	SA 10	SA 09	SA 08	SA 07	SA 06	SA 05	SA 04	SA 03	SA 02	SA 01	SA 00

ITSAR is a read/write register.

ITSAR<00-15>

Source low order address bits.

SOURCE MEMORY ADDRESS EXTENSION REGISTER (ITSXR)

15												03	02	01	00
												SA 19	SA 18	SA 17	SA 16

ITSXR is a read/write register.

ITSXR<00-03>

Source address bits 16-19.

An extra four bits are implemented in models with parity memory.
Source address bits 16-23.

15							07	06	05	04	03	02	02	00
							SA 23	SA 22	SA 21	SA 20	SA 19	SA 18	SA 17	SA 16

DESTINATION MEMORY ADDRESS REGISTER (ITDAR)

15															00
DA 15	DA 14	DA 13	DA 12	DA 11	DA 10	DA 09	DA 08	DA 07	DA 06	DA 05	DA 04	DA 03	DA 02	DA 01	DA 00

ITDAR is a read/write register.

ITDAR<00-15>

Destination low order address bits.

DESTINATION MEMORY ADDRESS EXTENSION REGISTER (ITDXR)

15												03	02	01	00
												DA 19	DA 18	DA 17	DA 16

ITDXR is a read/write register.

ITDXR<00-03>

Destination address bits 16-19.

An extra four bits are implemented in models with parity memory.
Destination address bits 16-23.

15							07	06	05	04	03	02	01	00
							DA 23	DA 22	DA 21	DA 20	DA 19	DA 18	DA 17	DA 16

TRANSFER COUNT REGISTER (ITTCR)

15															00
TC 15	TC 14	TC 13	TC 12	TC 11	TC 10	TC 09	TC 08	TC 07	TC 06	TC 05	TC 04	TC 03	TC 02	TC 01	TC 00

ITTCR is a read/write register.

ITTCR<00-15>

Size of operation, in words. Twos complement.

FUNCTION REGISTER (ITFR)

This dual purpose register functions as a command select and initialise on write, and as a memory size indicator on read. As a command register, bits 02 and 03 only are significant, and function as modified by bit 01 of ITCSR according to the following table:

ITFR			ITCSR		
Bit 3	Bit 2	Bit 1			
1	1	0	Buffer Init	)	MEMORY TEST
1	1	1	'Well Test'	)	
0	1	0	Forward	)	BLOCK MOVE
0	1	1	Backward	)	

On models with parity memory, bits 00 and 01 are significant, and function as modified by bit 01 of ITCSR according to the following table:

ITFR		ITCSR		
Bit 1	Bit 0	Bit 1		
0	1	0	Forward	BLOCK MOVE
0	1	1	Backward	BLOCK MOVE
1	0	0	Buffer Init	MEMORY TEST
1	0	1	'Well Test'	MEMORY TEST

BLOCK MOVE

The iterator will perform block moves, either in a forward or backwards direction according to Bit 1 in ITCSR. If Bit 1 is set to zero, the block moves in a forward direction and if set to 1, a backwards move.

All source and destination addresses, the block size, and ITCSR must be set up before the function is initiated by the appropriate bits in ITFR.

MEMORY TEST

This function is either to initialize blocks of memory to any data value preset in register ITDAR, or to perform "well" type tests.

A 'well test' is performed in two stages. First, the block of memory is set to all ones by the above 'buffer init' function and then the "well test" is initiated on the same block. This procedure first tests a word to see that it contains all ones, sets the word to all zeros and then tests that it is zero. This is repeated for all words in the block.

This test gives the memory a 'worst case' test by filling with all ones then all zeros and as it is implemented in microcode, is very fast.

As a memory size indicator, ITFR displays the number of 32 kilobyte blocks of memory implemented on the system as follows:

Memory Size	ITFR Contents
64 Kb	002
128 Kb	004
256 Kb	010
512 Kb	020
1 Mb	040
2 Mb	100
4 Mb	200

CONTROL AND STATUS REGISTER (ITCSR)

15	07	06	05	04	03	02	01	00
	RDY 07	IE 06	0	0	0	0	FCT 01	0

ITCSR is a read/write register.

ITCSR<01> - Function (FCT)

This bit has different meanings according to the functions to be performed. (Refer to ITFR charts)

ITCSR<06> - Interrupt Enable (IE)

Interrupt enable bit.

ITCSR<07> - Ready (RDY)

Ready, operation complete.

An extra bit is implemented in models with parity memory.

15	07	06	05	04	03	02	01	00
PE	RDY	IE	0	0	0	0	FCT	0

ITCSR<15> - Parity Error (PE)

This bit is set when a memory parity error is detected during an iterator function. It is cleared when a new iterator function is started, or by INIT.

INTRODUCTION

The Webster Electronics Floppy Disk controller is in two parts; the GPMI interface which handles the data flow between the floppy disk and memory, and the Western Digital FD1781 Floppy Disk controller chip which manages the actual disk drive.

9.1 DEVICE REGISTERS

Altogether there are nine device registers.

9.1.1 FD1781 Registers

FD1781 registers are all 8-bit.

DATA REGISTER (FDDR)

This register is used as a holding register (one's complement) during Disk Read and Write operations. When executing the Seek command, the Data Register holds the track of the desired Track position.

TRACK REGISTER (FDTR)

This register holds the one's complement of the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write and Verify operations. This register should not be loaded when this device is busy.

SECTOR REGISTER (FDSR)

This register holds the one's complement of the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. This register should not be loaded when the device is busy.

COMMAND/STATUS REGISTER (FDCSR)

This register (holding the one's complement) can be read or written via program control and as such is used to store the current disk command function code and operational status of the controller. This

register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt.

This device will accept and execute the following eleven commands -

FDCSR (WRITE)

Command	Definition
RESTORE	Move heads to track zero;
SEEK	Move heads from FDTR location to FDDR value;
STEP	Step heads one track in previous direction;
STEPIN	Step heads to next higher track;
STEPOUT	Step heads to next lower track;
READ	Find sector, read into core;
WRITE	Find sector, write core to disk;
READADR	Read 6 byte ID field from next sector;
FORCE	Terminate command, force type 1 status;
READTK	Read track from index to index;
WRITETK	Write track from index to index.

Command modifiers are applicable and relate to the 'Type' of command. Explicit details are contained in the 'Disk Command' section of this chapter.

FDCSR (READ)

BSY	Busy, command in progress;
IDX	Physical index (Type 1 command);
DRQ	Data Register flag (data transfer request);
TKO	Track zero status of selected unit;
LDT	Lost data byte (error condition);
CRC	Cyclic redundancy check error;
SKR	Seek error (Type 1 commands);
HNF	Header ID not found (READADR command);
RNF	Record not found (R/W commands);
HLD	Head loaded (Type 1 commands);
WRF	Write fault (WRITE command);
WRP	Write protect status of selected unit;
DDM	Deleted data mark (READ command);
NRY	Not ready status of selected unit.

9.1.2 GPMI Registers

The following registers are contained in the GPMI.

SELECT REGISTER (FDSEL)

This 16-bit Write only register selects the floppy disk drive number (0-3), the head (0, 1) and if double density.

15												03	02	01	00
												DDEN	HD	DS1	DS0

FDSEL<00-01> - Drive Select (DS0-DS1)

The drive select bits are configured 0-1 with the unit number of the drive to be currently selected.

FDSEL<02> - Head Select (HD)

Applicable to double sided, double density models only (C and D). If Bit 02 is cleared, selects Head zero. If Bit 02 is set, selects Head one.

FDSEL<03> - Double Density (DDEN)

Applicable to models C and D only (M-Board interface). Set for double density, cleared for single density.

CONTROL REGISTER (FDCTRL)

This register sets the data direction, ie., whether into or out of memory; whether the operation is to interrupt on completion; and one Ready status bit.

15									07	06					01	00
									RDY	IE					DD	

FDCTRL<01> - Data Direction (DD)

Read operation if Bit 01 is cleared. Write operation if Bit 01 is set.

FDCTRL<06> - Interrupt Enable (06)

Enables interrupt on completion.

FDCTRL<07> - Ready (RDY)

Ready, operation complete.

An extra bit is implemented in models with parity memory.

15							07	06					01	00
PE							RDY	IE					DD	

FDCTRL<15> - Parity Error (PE)

This bit is set when a memory parity error is detected during a write to disk. It is cleared whenever a command is issued to the floppy disk, or by INIT.

MEMORY ADDRESS REGISTER (FDMAR)

This 16-bit register contains the memory address of the data to be transferred.

15															00
MA 15	MA 14	MA 13	MA 12	MA 11	MA 10	MA 09	MA 08	MA 07	MA 06	MA 05	MA 04	MA 03	MA 02	MA 01	MA 00

FDMAR<00-15>

Memory low order address bits

MEMORY ADDRESS EXTENSION REGISTER (FDMXR)

For large memories, ie., those over 64Kb, FDMAR does not give enough addressing capability. FDMXR adds two bits to give 18 bits of address (256Kb) for the Floppy Disk transfers.

15														01	00
														MA 17	MA 16

FDMXR<00-01>

Memory address bits 16 and 17.

For systems with parity memory FDXMR contains eight memory address extension bits which in conjunction with FDMAR gives 24 bit addressing.

15								07	06	05	04	03	02	01	00
								MA 23	MA 22	MA 21	MA 20	MA 19	MA 18	MA 17	MA 16

TRANSFER COUNT REGISTER (FDTCR)

This 16-bit register counts the number of bytes transferred between Floppy Disk and memory.

15															00
TC 15	TC 14	TC 13	TC 12	TC 11	TC 10	TC 09	TC 08	TC 07	TC 06	TC 05	TC 04	TC 03	TC 02	TC 01	TC 00

FDTCR<00-15>

Size of transfer, in bytes. Twos complement.

9.2 DISK COMMAND DESCRIPTIONS

Command words should only be loaded in the Command Register when the Busy status bit is off. The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. To

facilitate the documentation of these commands, they have been divided into four types. The commands and types are summarized in Table 9-1, with a Flag Summary displayed for each Type (Tables 9 - 2/3/4/5).

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r1	r0
I	Seek	0	0	0	1	h	V	r1	r0
I	Step	0	0	1	u	h	V	r1	r0
I	Step in	0	1	0	u	h	V	r1	r0
I	Step Out	0	1	1	u	h	V	r1	r0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a1	a0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	s/
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I3	I2	I1	I0

Table 9-1 Command Summary

TYPE I

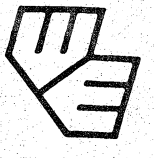
h = Head Load flag (bit 3)
h=1, Load head at beginning
h=0, Do not load head at beginning

V = Verify flag (Bit 2)
V=1, Verify on last track
V=0, No verify

r1r0 = Stepping Motor Rate (Bits 1-0)
Refer to Table 9-6 for rate summary

u = Update flag (Bit 4)
u=1, Update track register
u=0, No update

TABLE 9-2



10 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input every 10 msec. A low logic state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded before stepping to the destination track on the disk whenever the h bit is a logic zero.

9.2.1 Status Description

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt command is received when there is a current command under execution, the Busy Status bit is reset while the rest of the Status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the status bits is shown in Figure 9-1.

7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Figure 9-1 - Status Register

Status varies according to the type of command executed (Table 9-7).

BIT	ALL TYPE 1 COMMANDS	READ ADDR	READ	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROT	0	RECORD TYPE	WRITE PROT	WRITE PROT
S5	HEAD ENGAGED	0	RECORD TYPE	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY

Table 9-7

9.2.2 Command Types

TYPE I COMMANDS

The Type I (head positioning) commands include the Restore, Seek, Step, Step-in and Step-out commands.

r0r1

Each of the Type I commands contain a rate field (r0r1) which determines the stepping motor rate as defined in Table 9-6.

h

The Type I commands contain a Head Load flag (h) which determines if the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command (HLD output is made active). If h=0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the device controller (FD1781) receives a command that specifically disengages the head. If the FD1781 does not receive any commands after two revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 10msec delay, when reading or writing on the disk is to occur.

V

The Type I commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed, if V=0, no verification is performed. During verification, the head is loaded and after an interval of 10 msec delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is a valid ID CRC, an interrupt is generated, the Seek Error status bit (Status Bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status Bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after two revolutions of the disk, the FD1781 terminates the operation and sends an interrupt (INTRQ).

u

The Step, Step-in and Step-out commands contain an update flag (u). When u=1, the track register is updated by one for each step. When u=0, the track register is not updated.

RESTORE (SEEK TRACK 0)

Upon receipt of this command, the Track 00 (TR00/) input is sampled. If TR00/ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeros and an interrupt is generated. If TR00/ is not active low, stepping pulses (pins 15 to 17) at a rate specified by the r1r0 field are issued until the TR00/ input is activated. At this time the TR is loaded with zeros and an interrupt is generated. If the TR00/ input does not go low after 255 stepping pulses, the FD1781 terminates operation, interrupts and sets the Seek error status bit. Note that the Restore command is executed when MR (Master Reset) goes from an active to an inactive state. A verification operation takes place if the v flag is set; the h bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the track register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1781 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD1781 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD1781 issues one stepping pulse in the direction towards track 76 (WEBSTER format - track 77). If the u flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD1781 issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Status Bits for Type I Commands

S7 NOT READY

This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.

S6 PROTECTED

When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT/ (Write Protect) input.

S5 HEAD LOADED

When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.

S4 SEEK ERROR

When set, the desired track was not verified.
This bit is reset to 0 when updated.

S3 CRC ERROR

When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.

S2 Track 00

When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the TR00/ input.

S1 INDEX

When set, indicates index mark detected from drive. This bit is an inverted copy of the IP/ (Index Pulse) input.

S0 BUSY

When set, command is in progress. When reset, no command is in progress.

TYPE II COMMANDS

The Type II commands include the Read Sector(s) and Write Sector(s) commands. Prior to loading the Type II command into the Command Register, the processor must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy status bit is set. If the E flag = 1 (this is the normal case), HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is 0, the head is assumed to be engaged and there is no 10 msec delay. When an ID field is located on the disk, the FD1781 compares the Track number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from; depending upon the command. The FD1781 must find an ID field with a Track number, Sector number and CRC within two revolutions of the disk otherwise the Record Not Found status bit is set (Status Bit 3) and the command is terminated with an interrupt.

Each of the Type II commands contains a (b) flag which, in conjunction with the sector length field contents of the ID, determines the length (number of characters) of the Data field.

For IBM/DEC compatibility, the b flag should equal 1. The number of bytes in the data field (sector) is then 128 x 2n, where n = 0, 1, 2 or 3.

For b = 1

Sector Length Field (hex)	Number of bytes in sector (decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field.

For b = 0

Sector Length Field (hex)	Number of bytes in sector (decimal)
01	16
02	32
03	48
04	64
.	.
.	.
.	.
FF	4080
00	4096

Each of the Type II commands also contains an m flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record.

The FD1781 will continue to read or write mulltiple records and update the sector register until the register exceeds the number of sectors on the track or, until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

READ

Upon receipt of the Read command, the head is loaded, the Busy status bit is set and when an ID field is encountered that has the correct track number, correct sector number and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the corrected field; if not, the Record Not Found bit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR (Data Request), and DRQ is generated.

When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred, that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been

input. If there is a CRC error at the end of the data field, the CRC error status bit is set and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status register (Bits 5 and 6). Refer to Table 9-8.

STATUS BIT 5	STATUS BIT 6	DATA 1	DATA 2	DATA 3
0	0	0	0	0
0	1	0	0	1
1	0	0	1	0
1	1	0	1	1

TABLE 9-8

WRITE

Upon receipt of the Write command, the head is loaded (HLD active) and the Busy Status bit is set. When an ID field is encountered that has the correct track number, correct sector number and correct CRC, a DRQ is generated. The FD1781 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ ia serviced (ie., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a1a0 field of the command. Refer Table 9-9.

a1	a0	DATA 1	DATA 2	DATA 3
0	0	0	0	0
0	1	0	0	0
1	0	1	1	0
1	1	0	1	1

TABLE 9-9

The FD1781 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data Status bit is set and a byte of zeros is written to disk. The command is not terminated. After the last data byte has been written to disk, the two-byte CRC is computed internally and written to disk, followed by one byte gap of logic ones. The WG output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status bit is set. The next encountered ID field is then read in from the disk, the six data bytes of the ID field are assembled and transferred to the DR and a DRQ is generated for each byte. The six bytes of the ID field are shown in Figure 9-2.

TRACK ADDR	ZEROS	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Figure 9-2 - ID Field

Although the CRC characters are transferred to the computer, the FD1781 checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the Sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled, it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If Bit 0 (s) of the command is 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered, the operation is terminated making the device Not Busy, the Lost Data Status Bit is set and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream. (Refer Table 9-10). The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.

Control Bytes for Initialization

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK* (HEX)
F7	Write CRC character	FF
F8	Data Address Mark	C7
F9	Data Address Mark	C7
FA	Data Address Mark	C7
FB	Data Address Mark	C7
FC	Index Address Mark	D7
FD	Spare	
FE	ID Address Mark	C7

* Single Density only

DATA 1	DATA 2	DATA 3	TYPE OF ADDRESS MARK
0	0	0	Deleted Data mark
0	0	1	Data Mark (user defined)
0	1	0	Data Mark (user defined)
0	1	1	Data Mark
1	0	0	Index Address Mark
1	0	1	Undefined
1	1	0	ID Address Mark
1	1	1	Undefined

TABLE 9-10

Status Bits for Type II and Type III Commands

S7 NOT READY

This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III commands will not execute unless the drive is ready.

S6 RECORD TYPE/WRITE PROTECT

On Read Record: It indicates the MSB of record type code from data field address mark. On Read Track: Not used. On any Write: It indicates a Write fault. This bit is reset when updated.

S5 RECORD TYPE/WRITE FAULT

On Read Record: It indicates the LSB of record type code from data field address mark. On Read Track: Not Used. On any Write: It indicates a Write Fault. This bit is reset when updated.

S4 RECORD NOT FOUND

When set, it indicates that the desired track and sector were not found. This bit is reset when updated.

S3 CRC ERROR

If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.

S2 LOST DATA

When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.

S1 DATA REQUEST

This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.

S0 BUSY

When set, command is under execution. When reset, no command is under execution.

TYPE IV COMMAND

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I0 through I3 field is detected.

If the I0I3 field = 0, there is no interrupt generated but the current command is terminated and Busy is reset.

9.3 DATA FORMAT

When diskettes are obtained, they are normally blank or in a type of format which is not suitable for Spectrum Eleven computers. Hence, every disk has to be formatted in a native form suitable for the type of device storage used.

A Spectrum machine is capable of accepting several formats -

DX	DEC/IBM format single density 76 track;
1S	WEBSTER format single density 77 track;
1D	WEBSTER format double density 77 track;
2D	WEBSTER format double density dual head 77 track.

WEBSTER formats have been established to make floppy disk systems a more cost effective computer/storage system. Careful planning of format layouts increases access, performance and storage space.

In order to format disks in non-DEC layout, FUTIL (Floppy UTILity) must be used. For instructions on the use of FUTIL, refer to Spectrum Eleven RT-11 Software Manual.

INTRODUCTION

This chapter discusses the software interface for the disk controller including device registers and their addresses, the interrupt process, timing considerations and data format.

10.1 DEVICE REGISTERS

The controller software communication is accomplished by seven device registers. These registers are assigned memory addresses and can be read or written into (except where noted) using instructions that refer to the respective register addresses. Transfers to these registers may be made as full words or as bytes. Unassigned and write-only bits are always read as zeros. Any attempt to manipulate unassigned or read-only bits has no effect. Refer Table 10-1 for details of these 7 registers.

REGISTER NAME	MNEMONIC	ADDRESS	TYPE
Drive Status	RKDS	777400	Read Only
Error	RKER	777402	Read Only
Control Status	RKCS	777404	Read/Write
Word Count	RKWC	777406	Read/Write
Bus Address	RKBA	777410	Read/Write
Disk Address	RKDA	777412	Read/Write
Data Buffer	RKDB	777416	Read/Write

Table 10-1 Device Registers

NOTE:

Address 777414 is not implemented but will respond with all zeros if a read is attempted. A Write operation will result in a reply to the computer but will have no effect on the controller.

DRIVE STATUS REGISTER (RKDS)

The RKDS register (Figure 10-1) is a read-only register containing status of the selected drive.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ID 2	ID 1	ID 0	DPL	RK05	DRU	SIN	SOK	DRY	R/W/S RDY	WPS	SC=SA	SC 3	SC 2	SC 1	SC 0

Figure 10-1 Drive Status Register (RKDS)

RKDS<00-03> - Sector Counter (SC)

These four bits contain the current sector address of the selected drive. Sector address 0 is defined as the sector following the sector that contains the index pulse.

RKDS<04> - Sector Counter Equals Sector Address (SC=SA)

When set, indicates that the disk heads are positioned over the disk address currently held in the sector address field (SA) of RKDA. Ie., SC = SA.

RKDS<05> - Write Protect Status (WPS)

When set, indicates that the selected disk is in the write-protected mode.

RKDS<06> - Ready/Write/Seek/Ready (R/W/S/RDY)

When set, indicates that a Seek or Drive Reset function is not in process and that the drive is ready to accept a new function.

RKDS<07> - Drive Ready (DRY)

When set, indicates that the disk drive complies with all the following conditions.

The drive is properly supplied with power;
The drive is loaded with a disk cartridge;
The disk drive door is closed;
The LOAD/RUN switch is set to RUN;
The disk is rotating at a proper speed;
The heads are properly loaded;
The disk is not in an unsafe condition, ie., Drive Unsafe (DRU), bit 10 in RKDS is not set.

RKDS<08> - Sector Counter OK (SOK)

When set, indicates that the Sector Counter (SC) is not in the process of changing and is ready for examination. If this bit is not set, the Sector Counter is not ready for examination and a later attempt should be made to read SC.

RKDS<09> - Seek Incomplete (SIN)

When set, indicates that due to some unusual condition, a Seek function cannot be completed. May be accompanied by Drive Error (DRE), bit 15 in RKER. Cleared by a Drive Reset function.

RKDS<10> - Drive Unsafe (DRU)

When set, indicates that an unusual condition has occurred and that the disk drive is unable to properly perform any operations. This bit is reset by setting the drive RUN/LOAD switch to LOAD. If the bit is again set when the switch is returned to RUN, it should be assumed that the drive is inoperative and in need of maintenance. May be accompanied by Drive Error (DRE), bit 15 in RKER.

RKDS<11> - RK05 Disk on Line (RK05)

Always set to identify the selected disk as being RK05 compatible.

RKDS<12> - Drive Power Low (DPL)

Monitors the state of the bus ac power status (BPOKH) and sets DPL if BPOKH is in the unasserted state.

RKDS<13-15> - Identification of Drive (ID)

If an interrupt occurs, these bits will contain the binary representation of the logical drive number that caused the interrupt.

ERROR REGISTER (RKER)

The RKER register (Figure 10-2) is a read-only register containing all error status indicators for the selected drive.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DRE	OVR	WLO	SKE	PGE	NXM	DLT	TE	NXD	NXC	NXS				CSE	WCE

Figure 10-2 Error Register (RKER)

RKER<00> - Write Check Error (WCE)

When set, indicates that an error was encountered during a Write Check function as a result of a faulty bit comparison between disk data and memory data. Reset by the initiation of a new function. This is a soft error condition.

RKER<01> - Checksum Error (CSE)

When set, indicates that an error was encountered while performing a Read Check or a Read function as a result of a mismatch between the checksum read from disk and that calculated by the controller. Reset by the initiation of new function. This is a soft error condition.

The remaining bits of this RKER register are all hard errors and are cleared only by a BUS INIT or a Control Reset function.

RKER<05> - Nonexistent Sector (NXS)

When set, indicates that an attempt was made to initiate a transfer to a sector number larger than 13 (octal).

RKER<06> - Nonexistent Cylinder (NXC)

When set, indicates that an attempt was made to initiate a transfer to a cylinder number larger than 312 octal.

RKER<07> - Nonexistent Disk (NXD)

When set, indicates that an attempt was made to initiate a function on a nonexistent or not ready drive.

RKER<08> - Timing Error (TE)

When set, indicates a loss of drive read clock has been detected.

RKER<09> - Data Late (DLT)

Set during a Write or Write Check function if the multibuffer file (FIFO) is empty at the time a write clock occurs. Set during a Read function if the multibuffer file (FIFO) is filled at the time a read clock occurs.

RKER<10> - Nonexistent Memory (NXM)

Set if memory does not respond with REPLY within 10 microseconds after the controller becomes bus master during a DMA sequence. Because of the speed of the disk drive, it is possible that NXM will be accompanied by Data Late, bit 9 of RKER.

RKER<11> - Programming Error (PGE)

When set, indicates that Format, bit 10 of RKCS, was set while initiating a function other than Read or Write.

RKER<12> - Seek Error (SKE)

Set if the disk head mechanism is not properly positioned while executing a normal Read, Write, Read Check or Write Check function. The controller checks sector address 16 times before flagging this error.

RKER<13> - Write Lockout Violation (WLO)

Set if an attempt is made to write on a disk that is currently write-protected.

RKER<14> - Overrun (OVR)

When set, indicates that during a Read, Write, Read Check or Write Check function, operations in sector number 13 (octal), surface number 1 (bottom), of cylinder address number 312 (octal) were finished and the RKWC has not yet overflowed. This error flags an attempt to overflow out of a logical disk drive.

RKER<15> - Drive Error (DRE)

Set if a function is either initiated or is in process when the selected drive is either not ready or is in some error condition.

CONTROL STATUS REGISTER (RKCS)

The RKCS register (Figure 10-3) is a read/write register which holds control codes to the controller supplied by the computer and the current state of these control codes, plus control status generated in the controller. Some bits are read only and some are write only as defined below.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	HE	SCP			IBA	FMT		SSE	RDY	IDE	MEX	MEX	F3	F2	F1	GO

Figure 10-3 Control Status Register (RKCS)

RKCS<00> - Go (GO)

Loaded by the program. When set, causes the controller to execute the function contained in bits 01 through 03 of RKCS. Remains set until the controller actually responds to GO, which may take from 1 microsecond to 3.3 milliseconds depending on the current operation of the selected disk drive; reset when execution is initiated.

RKCS<01-03> - Function Code (F1-F3)

Loaded by the program with the binary representation of the function to be performed by the controller when the GO command is initiated, reset by BUS INIT. The function is retained until altered by the program or cleared, enabling the user to continue from a soft error condition with GO. The configuration of the Function Code bits (F1-F3), with the setting of the GO bit, allows the selected drive to respond to the following commands:

Command	F3	F2	F1	GO	Octal
Control Reset	0	0	0	1	01
Write	0	0	1	1	03
Read	0	1	0	1	05
Write Check	0	1	1	1	07
Seek	1	0	0	1	11
Read Check	1	0	1	1	13
Drive Reset	1	1	0	1	15
Write Lock	1	1	1	1	17

RKCS<04-05> -Memory Extension (MEX)

Reserved for extended bus addresses used in conjunction with the RKBA. This 2-bit counter increments each time the RKBA overflows. A bus DATO to these bits overrides an RKBA overflow. Loaded by the program and cleared by BUS INIT. Use of these bits is intended for systems which are equipped with a memory larger than 64K bytes.

RKCS<06> - Interrupt on Done Enable (IDE)

When set causes the control to issue a bus interrupt request and interrupt to vector address 220 (octal) if:

A function has completed activity;

A hard error is encountered;

A soft error is encountered and Stop on Soft Error (SSE), bit 8 of RKCS is set.

The Control Ready (RDY), bit 7 of RKCS, is set and GO is not set.

RKCS<07> - Control Ready (RDY)

When set, indicates that the controller is ready to perform a function. Set by INIT, a hard error condition or by the termination of a function. Cleared when GO is set.

RKCS<08> - Stop on Soft Error (SSE)

If a soft error is encountered when this bit is set:

If Interrupt on Done Enable (IDE), bit 6 of RKCS, is reset, all control action will stop at the end of the current sector.

If IDE is set, all control action will stop and a bus interrupt request will occur at the end of the current sector.

RKCS<10> - Format (FMT)

FMT is under program control and must be used only in conjunction with normal Read and Write functions. Used to format a new disk pack or to reformat any sector erased due to the controller or drive failure. Alters the normal Write operation, under which the header is rewritten each time the associated sector is rewritten, in that the head positioner is not checked for proper positioning before the Write. Alters the normal Read operation in that only the header word is transferred to memory out of each sector read from disk. Header words from contiguous sectors will be read into contiguous memory locations.

RKCS<11> - Inhibit Incrementing the RKBA (IBA)

Inhibits the RKBA from incrementing during a normal function. This allows data transfers to occur to or from the same memory location throughout the entire operation.

RKCS<13> - Search Complete (SCP)

When set, indicates that the previous interrupt was the result of some previous Seek or Drive Reset function. Cleared at the initiation of any new function.

RKCS<14> - Hard Error (HE)

Set when bits 5-15 of RKER are set and stops all control action. Processor reaction is dictated by the state of bit 6 (IDE) in RKCS until this bit along with bits 5-15 of RKER, are all cleared either by INIT or a Control Reset function.

RKCS<15> - Error (ERR)

Set when any bit of the RKER is Set. Processor reaction is dictated by the states of bit 6 (IDE) and bit 8 (SSE) in RKCS. Cleared if all bits in the RKER are cleared.

WORD COUNT REGISTER (RKWC)

15															00
WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 09	WC 08	WC 07	WC 06	WC 05	WC 04	WC 03	WC 02	WC 01	WC 00

Figure 10-4 Word Count Register (RKWC)

The RKWC register (Figure 10-4) is loaded by the program initially with the two's complement of the total number of words to be affected or transferred by a given function. The controller increments this register by one after each word transfer. When the register overflows (all WC bits go to zero), the transfer is complete and the operation is terminated at the end of the present disk sector. However, only the number of words specified in the RKWC are transferred.

CURRENT BUS ADDRESS REGISTER (RKBA)

15															00
BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 09	BA 08	BA 07	BA 06	BA 05	BA 04	BA 03	BA 02	BA 01	BA 00

Figure 10-5 Current Bus Address Register (RKBA)

The bits in this RKBA register (Figure 10-5) specify the bus address to or from which the next data word will be transferred. The register is incremented by two at the end of each transfer. If the system has extended memory, the RKBA will overflow to the MEX (bits 4 and 5 of the RKCS) to reflect the extended bus addresses.

DISK ADDRESS REGISTER (RKDA)

DS 2	DS 1	DS 0	CA 7	CA 6	CA 5	CA 4	CA 3	CA 2	CA 1	CA 0	SUR	SA 3	SA 2	SA 1	SA 0

Figure 10-6 Disk Address Register (RKDA)

This register (Figure 10-6) will not respond to write commands from the processor while the controller is busy. Therefore, RKDA bits may be loaded from the bus data lines only when the Control Ready (RDY), bit 7 of RKCS, is set. The register is cleared by BUS INIT or Control Reset.

RKDA<00-03> -Sector Address (SA)

Loaded initially by the program. Holds the disk sector to be addressed for the next operation. During operations, SA is incremented after each sector and counts modulus 14 (octal). If SA is initially loaded with a number greater than 13 (octal) and an operation is initiated (GO), a hard error occurs and bit 5 (NXS) of RKER is set.

RKDA<04> - Surface (SUR)

When set, selects the lower surface disk head; when reset, selects the upper surface disk head. This bit is automatically toggled by the controller at the end of each track.

RKDA<05-12> - Cylinder Address (CYL ADDR)

Loaded initially by the program. Holds the cylinder currently being selected. During operation, CYL ADDR is incremented after each cylinder and counts modulas 313 (octal). If CYL ADDR is initially loaded with a number greater than 312 (octal) and an operation is initiated (GO set), a hard error occurs and bit 6 (NXC) of RKER is set.

RKDA<13-15> - Drive Select (DR SEL)

Binary representation of the logical unit number currently being selected. The eight logical units are mapped on to the four physical platters of the single physical drive. Unit 0 is recorded at 100 tpi on both sides of the removable platter in a manner compatible with

standard DEC RK05 media. Unit 1 is recorded interleaved between the tracks of unit 0, resulting in a net track density of 200 tpi. The remaining six logical units are distributed in like fashion over the three fixed platters.

DATA BUFFER REGISTER (RKDB)

15															00
DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 09	DB 08	DB 07	DB 06	DB 05	DB 04	DB 03	DB 02	DB 01	DB 00

Figure 10-7 Data Buffer register (RKDB)

All data words transferred between the controller and the disk drive(s) pass through the RKDB register (Figure 10-7). Is loadable from the computer only via the bus while the controller is bus master during the DMA sequence, ie., cannot be loaded directly by the program but can be read by the program.

10.2 DATA FORMAT

This section defines the data formats as written and recovered by the controller.

Data is stored on the disk cartridge in groups of 12 sectors per track. Each sector contains 256 data words and is defined by a sector mark which generates a sector pulse. All sectors are formatted identically in five parts; preamble (terminated with a sync bit), header, data, checksum and postamble as displayed in Figure 10-8. Each word (excluding sync) is 16 bits.

Preamble	SYNC	Header	Data	Checksum	Postamble
Zeros (13 Words)	1 (1 bit)	Cylinder Address (1 Word)	(256 Words)	Sector Checksum (1 Word)	Zeros (1 Word)

----------> Reading Direction

Figure 10-8 Data Format

The preamble and postamble areas of a sector serve as boundaries surrounding the information words (header, data and checksum) to ensure compatibility between disk drives at the cartridge level despite variations in sector pulse positioning.

The preamble consists of 13 words of zeros to insure that the data read circuitry in the drive will lock on during a known zero data field. For a Read operation, the controller waits for the sync bit to occur and then begins to read with the header word. For a Write function, the sync bit is automatically written by the controller following 13 words of zeros.

The header area of a sector consists of a single word containing the cylinder address. Before a data transfer function is performed, the header word is read and checked against the cylinder address portion of the RKDA to ensure that the disk drive heads are positioned above the proper cylinder. The Write function always rewrites the header on the disk, using the cylinder address portion of the RKDA. The sector format for an unformatted cartridge is written under program control in conjunction with bit 10 (FMT) of RKCS.

The data area consists of 256 data words, 16 bits per word. The checksum area of a sector consists of a single word that is the checksum of all 256 data words. This recorded checksum is compared by the controller to a computed checksum whenever a Write Check, Read, or Read Check function is performed within a given sector. For a Write function, the controller calculates a checksum and writes it on the disk cartridge following the last data word of a sector.

Short portions (less than 256 data words) of a sector may be read or written as long as this short sector is the last sector of the data transfer. When a short sector is written, the remainder of the sector is automatically written with zeros. The Write Check function may be performed on a short sector as long as the number of words write checked is equal to the number of words previously written into the sector. Because the Read Check function is essentially a parity check, it must be performed on a whole-sector basis only.

INTRODUCTION

All data transfers use the GPMI for a direct access to main memory, at a maximum transfer rate of up to 520,000 words per second (1.9 microseconds per word), in block sizes ranging from 1 to 65,536 words. To achieve a smooth flow of data from disk to main memory, the subsystem utilizes a first in/first out, 16 byte data buffer known as a Silo. Upon the indication of an error condition or the completion of a command, the controller can interrupt the processor. Extensive error indicators exist for on-line diagnosis, while numerous status indicators provide complete program control.

The following paragraphs provide detailed descriptions of controller register content and usage, followed by disk command descriptions and programming considerations related to the use of the Winchester disk systems.

11.1 DEVICE REGISTERS

There are 10 usable 16-bit device registers (11 for models with parity memory), contained in the 'T' board controller, used to interface with the Winchester drives and Q-bus. These registers are loaded and/or read under program control to initiate selected disk commands and monitor subsystem status and error conditions. Device register bits are generally cleared by a Q-bus Initialize (INIT), Controller Clear (CCLR) or Subsystem Clear (SCLR) operation. In the following descriptions (unless otherwise specified), it should be understood that the clearing of a bit by any one of these three methods is implied.

NOTE:

The Controller does not recognize DATOB (MOVB, BICB, etc) bus cycles. All registers must be written as words.

CONTROL/STATUS REGISTER 1 (RKCS1)

The RKCS1 register (Figure 11-1) can be read or written by program control and is used to store the current disk command function code and operational status of the controller. In addition, the register can initiate command execution and enable a Controller Clear operation.

15	14	13	12	11	10	09*	08*	07	06	05	04	03	02	01	00
CERR	DI	0	0	0	CDT	BA17	BA16	RDY	IE	0	F4	F3	F2	F1	GO

Figure 11-1 Control Status Register 1 (RKCS1)

RKCS1<00> - Go(GO)

With the GO bit set, only two other device register bits can be set, as follows:

Controller Clear (CCLR), bit 15 in RKCS1, may be set via program control to initialize (general clear and preset) certain device registers within the controller. However, any status and/or error conditions set in the drives are not affected.

Subsystem Clear (SCLR), bit 5 in RKCS2, may be set via program control to initialize both the controller and all the drives.

When command execution is completed, the GO bit is reset and the controller is ready to accept a new command. However, the GO bit cannot be set if the Combined Error (CERR) bit is set. When CERR is set, the execution of a command can only occur following the initiation of a CCLR.

RKCS1<01-04> - Function Code (F1-F4)

The configuration of the Function Code bits (F1-F4), with the setting of the GO bit, allows the selected drive to respond to the following commands.

Command	F4	F3	F2	F1	GO	Octal
Select Drive	0	0	0	0	1	01
Set Status (NOP)	0	0	0	1	1	03
Drive Clear	0	0	1	0	1	05
Unload	0	0	1	1	1	07
Start Spindle	0	1	0	0	1	11
Recalibrate	0	1	0	1	1	13
Set Status (NOP)	0	1	1	0	1	15
Seek	0	1	1	1	1	17
Read Data	1	0	0	0	1	21
Write Data	1	0	0	1	1	23
Illegal cmd	1	0	1	0	1	25
Write Header	1	0	1	1	1	27
Write Check	1	1	0	0	1	31
Illegal cmd	1	1	0	1	1	33
Read Format	1	1	1	0	1	35
Illegal cmd	1	1	1	1	1	37

RKCS1<06> - Interrupt Enable (IE)

When the Interrupt Enable (IE) bit is set, the controller will be allowed to interrupt the processor under any of the following conditions:

When Controller Ready (RDY), bit 7 in RKCS1, is set upon completion of a command.

When the drive or the controller indicates the presence of an error by the setting of Controller Error (CERR), bit 15 in RKCS1.

Interrupt Enable, bit 6, can be reset via program control as well as by conventional initialization (INIT, CCLR, SCLR).

RKCS1<07> - Controller Ready (RDY)

Controller Ready (RDY) is effectively a read-only bit. However, the bit can be externally set via convential initialization (INIT, CCLR, SCLR) or internally set upon completion of a command. The RDY bit is reset when GO, bit 0 in RKCS1, is set.

RKCS1<08-09> - Extended Bus Address (BA16, BA17)

The Extended Bus Address bits reflect Q-bus upper address bits 16 and 17 and as such are an extension of the 16-bit RKBA register which contains the memory address required for the current data transfer.

* On systems with parity memory, these bits have no function.

RKCS1<10> - Controller Drive Type (CDT)

This bit specifies the type of drive that will be selected by the controller. To specify H Disk Drives, the bit must be reset. For G,J and K Drives, the bit must be 1.

RKCS1<14> - Drive Interrupt (DI)

In relation to program control, Drive Interrupt (DI) is a read-only bit. When set, the bit differentiates between a drive-initiated interrupt and a controller-initiated interrupt.

If the Interrupt Enable (IE) bit is set, the setting of the DI bit with the set condition of Controller Ready (RDY), bit 7 in RKCS1, indicates a drive-initiated interrupt. The DI bit is reset by Q-bus Initialize (INIT) or Subsystem Clear (SCLR).

RKCS1<15> - Combined Error/Controller Clear (CERR/CCLR)

As a combined Error (CERR) indicator, bit 15 can be set by the controller or the drive, to indicate that a subsystem error has occurred (Table 11-1). However, when the bit is set via program control, a controller initialize (CCLR) operation is enabled which clears the controller and results in the clearing of bit 15 itself. Thus, if the bit is internally set (CERR) by an error that is followed by an external set (CCLR) to initialize the controller, bit 15 will be cleared. As only controller errors are initialized by CCLR, any error originating in the drive will remain set in the drive.

When using a BIC instruction on the RKCS1 register, ensure that a 1 is set in bit 15 of the mask. If this is not done and CERR is set, a CCLR will occur and the controller will be cleared. For example, to clear Interrupt Enable (bit 6 in RKCS1), the following instruction format is advised:

```
BIC #100100,@RKCS1
```


Table 11-1 Combined Error (CERR)

Error	Indicator Bit / Condition
Programming Error (PGE)	RKCS2 bit 10 Register written (except CCLR,SCLR) with GO set.
Illegal Function (ILF)	RKER bit 0 Illegal command in low-order 5 bits of RKCS1.
Drive Type Error (DTE)	RKER in bit 5 CDT bit in RKCS1 does not match DDT bit in RKDS.
Cylinder Overflow (COE)	RKER bit 9 Cylinder address exceeded.
Invalid Disk Address (IDAE)	RKER bit 10 Invalid cylinder or track address detected.
Parity Error (PE)	RKCS2 bit 13 Implemented only on systems with parity memory.
Nonexistent Drive (NED)	RKCS2 bit 12 Drive response problem.
Drive Error (DRERR)	RKER bits 1, 11, 14 Any drive error condition.
Operation Incomplete (OPI)	RKER bit 13 Desired header cannot be found.
Write Check Error (WCE)	RKCS2 bit 14 Write check indicates data from disk did not match from memory.
Data Late Error (DLTERR)	RKCS2 bit 15 Data late to/from Silo.
Drive Timing Error (DTE)	RKER bit 12 Write clock loss during write, data loss during read.
Data Check (DCK)	RKER bit 15 Data error detected by CRC.
Error Correction Hard (ECH)	RKER bit 6 Data error not able to be corrected.

WORD COUNT REGISTER (RKWC)

The RKWC register (Figure 11-2) is loaded with the twos complement of the data words to be transferred to or from main memory. The register is incremented by 1 after each bus cycle and accommodates a maximum transfer of 65,536 words. The RKWC register can only be cleared by writing all zeros via program control.

15															00
WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 09	WC 08	WC 07	WC 06	WC 05	WC 04	WC 03	WC 02	WC 01	WC 00

Figure 11-2 Word Count Register (RKWC)

BUS ADDRESS REGISTER (RKBA)

The RKBA register (Figure 11-3) is initially loaded with the low-order 16 bits of the Q-bus address that will reflect the main memory start location for a data transfer. With the low-order bit(0) always forced to 0, the RKBA register content is combined with high-order bits 8 and 9 of RKCS1 register (BA16,17), or from RKBAX (BA16,17,18,19,20,21,22,23) in a system with parity memory, to form a complete even-numbered word address. Following each data transfer bus cycle, the register is incremented by two to select the next even-numbered location.

15															00
BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 09	BA 08	BA 07	BA 06	BA 05	BA 04	BA 03	BA 02	BA 01	BA 00

Figure 11-3 Bus Address Register (RKBA)

DISK ADDRESS REGISTER (RKDA)

For Read, Write and Write Check commands, the RKDA register (Figure 11-4) is initially loaded to define the desired sector (1 of 22) and track (1 of 3 read/write heads) on the selected unit from or to which the first block of a data transfer will be initiated. If the word count value indicates that a block of more than 256 data words is to be transferred, the Sector Address bits of the RKDA

register will be incremented to select the next consecutive sector and the next track, if necessary, until a word count overflow indicates that data transfers are completed or an error occurs. In either case, completion of the command is indicated by the setting of the Controller Ready (RDY) bit in RKCS1 and an increment of the RKDA register to the next sector location.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	TA 2	TA 1	TA 0	0	0	0	SA 4	SA 3	SA 2	SA 1	SA 0

Figure 11-4 Disk Address Register (RKDA)

RKDA<00-04> - Sector Address (SA0-SA4)

Sector Address 0-4 are configured (00-25) to select a value (o to 21 decimal) for a 22-sector format (16-bit data words). The Sector Address is incremented by one when the sector has been transferred.

RKDA<08-10> - Track Address (TA0-TA2)

The Track Address bits are configured (0-2) to select the appropriate read/write head associated with the desired track. After the last sector (25 octal) on the track has been transferred and the Sector Address has been reset to zero, the Track Address bits are incremented by one. Similarly, if transfers continue beyond the last sector of the last track (2) of a given cylinder, the Track Address is reset to zero and the Cylinder Address (in RKDC) is incremented by one. In this manner, subsequent sectors, tracks and cylinders can be consecutively transferred until the word count equals zero. However, if the word count does not equal zero after the transfer of the last sector (21 decimal) on the last track (2) of the last cylinder (252 decimal for an H subsystem, 874 decimal for a G subsystem,979 decimal for a J subsystem or 839 decimal for a K subsystem), a Cylinder Overflow Error (COE) will occur.

CONTROL/STATUS REGISTER 2 (RKCS2)

RKCS2 register (Figure 11-5) can be read or written via program control and is used to store the current drive select code, subsystem operational status and the Silo control information. In addition, the register can initiate a Subsystem Clear (SCLR) operation.

15	14	13*	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	PE	NED	0	PGE	0	0	0	0	SCLR	0	0	0	DS1	DS0

Figure 11-5 Control/Status Register 2 (RKCS2)

RKCS2<00-01> - Drive Select (DS0-DS1)

The Drive Select bits are configured 0-3 with the unit number of the drive to be currently selected.

RKCS2<05> - Subsystem Clear (SCLR)

When the SCLR bit is set via program control, the controller is cleared and the Initialise line is asserted on the drive interface to clear all of the drives available to the system.

RKCS2<10> - Programming Error (PGE)

Programming Error is a read-only error bit that is set if any controller register is written (bits for CCLR and SCLR excepted) while the GO bit in RKCS1 is set.

RKCS2<12> - Nonexistent Drive (NED)

Nonexistent Drive is a read-only error bit that is set to indicate the following:

The front panel access switch has been depressed, forcing the drive into an off-line condition.

The Drive Select bits (DS0,DS1 in RKCS2) imply a unit number greater than that specified by the configuration switch(es) on the controller.

RKCS2<13> - Parity Error (PE)

This is a read only error bit that is set to indicate that a memory parity error occurred during a write to disk.

* On systems without parity memory, this bit has no function.

RKCS2<14> - Write Check Error

Write check error is a read-only bit that is set to indicate that a data word read from the disk during the execution of a Write Check command did not compare with the corresponding data word contained in main memory.

RKCS2<15> - Data Late Error (DLT)

Data Late Error is a read-only error bit that is set to indicate the following:

During the execution of a Write or Write Check command, the Silo was empty when the disk required a data word.

During the execution of a Read command, the Silo was full when the disk provided the next data word.

DRIVE STATUS REGISTER (RKDS)

The RKDS register (Figure 11-6) is a read-only register that is used to store the operational status of a selected drive. However, information obtained from the drive is not immediately available to program control until the information is validated (SVAL) by the setting of bit 15 which indicates that a complete status image has been assembled providing a valid update.

Status information bits set in the RKDS register can be cleared by conventional initialization (INIT, CCLR, SCLR). However, a Controller Clear (CCLR) operation does not affect status or error condition bits that are currently set in the drive. In addition, a Q-bus Initialize (INIT) or Subsystem Clear (SCLR) operation can only reset status or error bits in a drive if the associated status or error condition no longer exists.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
SVAL	CDA	0	0	WRL	0	0	DDT	DRDY	VV	0	0	0	0	0

Figure 11-6 Drive Status Register (RKDS)

RKDS<06> - Volume Valid (VV)

Volume Valid is a read-only bit that is always set.

RKDS<07> - Drive Ready (DRDY)

Drive Ready is a read-only bit that is set to indicate that the selected drive is up to speed and the heads are properly positioned over a valid cylinder. Under these conditions, the drive is prepared to accept a command.

RKDS<08> - Disk Drive Type (DDT)

Disk Drive Type is a read-only bit that is internally conditioned to indicate the type of drive selected. For an H drive, the bit remains reset and for a G, J or K Drive, the bit is set. However, before any commands can be executed, the bit must compare with the condition of Controller Drive Type, bit 10 in RKCS1.

RKDS<11> - Write Lock (WRL)

Write Lock is a read-only bit that is set if the drive is write protected.

RKDS<14> - Current Drive Attention (CDA)

Current Drive Attention is a read-only bit that is set for any of the following conditions:

A seek fault occurred in the drive.

A seek operation is completed.

A command was rejected by the drive.

RKDS<15> - Status Valid (SVAL)

Status Valid is a read-only bit that is set to indicate that the bits in both the Drive Status (RKDS) and Error (RKER) registers have been updated for the drive. The bit is cleared by conventional initialization (INIT, CCLR, SCLR) or by initiating a new command (writing in RKCS1).

DRIVE ERROR REGISTER (RKER)

The RKER register (Figure 11-7) is a read-only register that is used to store the error status of the drive. However, error information obtained from the drive is not immediately available to program control until the information is validated (SVAL) by the setting of bit 15 in the RKDS register.

Error bits set in the RKER register can be cleared by conventional initialization (INIT, CCLR, SCLR). However a Controller Clear (CCLR) operation does not affect error bits that are currently set in the drive. In addition, a Q-bus Initialize (INIT) or Subsystem Clear (SCLR) operation can only reset error bits in the drive if the associated error condition no longer exists.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IDAE	COE	HVRC	BSE	ECH	DTYE	0	0	0	SKI	ILF

Figure 11-7 Drive Error Register (RKER)

RKER<00> - Illegal Function (ILF)

Illegal Function is a read-only bit that is set to indicate that an illegal command (25, 33, 37 octal) has been loaded into RKCS1.

RKER<01> - Seek Incomplete (SKI)

Seek Incomplete is a read-only bit that is set to indicate that a seek operation has not been completed for one of the following conditions:

A seek fault occurred in the drive.

A command was rejected by the drive.

RKER<05> - Drive-Type Error (DTYE)

Drive-Type Error is a read-only bit that is set when the drive-type (RKDS bit 8) does not compare with the CDT bit (bit 10) in RKCS1 (reset for subsystem H or set for subsystem G, J or K).

RKER<06> - Error Correction Hard (ECH)

Error Correction Hard is a read-only bit that is set to indicate a CRC error during a Read command. This sets RKER bit 15.

RKER<07> - Bad Sector Error (BSE)

Bad sector error is a read only bit which is set whenever an OPI (RKER13) error occurs.

RKER<08> - Header Vertical Redundancy Check Error (HVRC)

Header VRC error is a read only bit which is set whenever an OPI (RKER13) error occurs.

RKER<09> - Cylinder Overflow Error (COE)

Cylinder Overflow Error is a read-only bit that is set to indicate that the RKWC register is not equal to zero following a data transfer from cylinder 252 decimal (subsystem H), 874 decimal (subsystem G), 979 decimal (subsystem J) or 839 (subsystem K), track 2 and sector 21 (last logical sector).

RKER<10> - Invalid Disk Address (IDAE)

Invalid Disk Address is a read-only bit that can be set by the controller, to indicate the following:

The controller detected an illegal desired cylinder (DC0-DC9) value in the RKDC register during the initiation of a command;

The controller detected an illegal track address (TA0-TA2) value in the RKDA register during the initiation of a command.

RKER<11> - Write Lock Error (WLE)

Write-Lock Error is a read-only bit that is set to indicate that a Write or Write Header command commenced while the drive was in WRITE PROTECT mode. The occurrence of this fault allows the CDA bit to be set in RKDS.

RKER<12> - Drive Timing Error (DTE)

Drive Timing Error is a read-only bit that is set to indicate a sector overrun error, probably as a result of loss of serial clock or data signals from the drive.

RKER<13> - Operation Incomplete (OPI)

Operation Incomplete is a read-only bit that is set to indicate that following the positioning of the heads to a desired cylinder and the reading of 44 headers, the desired header could not be found. This error can result from any one of the following:

Head mispositioning;

Incorrect head selection;

Read channel failure;

Improper formatting;

Header checksum miss on desired sector.

RKER<14> - Drive Unsafe (UNS)

Drive Unsafe is a read-only bit that is set to indicate that any one of the following Read/Write Unsafe conditions has been detected.

WRITE GATE without write current at the head;

Write current at the head without WRITE GATE;

WRITE GATE without READY;

More than one head selected;

No transitions during write;

WRITE GATE with WRITE PROTECT;

Spindle Speed Error;

RESET while drive Sequenced Up;

Off-Track condition when track following (READY);

Failure to Restore;

Software Error (Watch-dog timer time out).

RKER<15> - Data Check (DCK)

Data Check is a read-only bit that is set to indicate that a data error was detected when the current sector was read.

ATTENTION SUMMARY REGISTER (RKAS)

The RKAS register (Figure 11-8) is a read only register which indicates the ready status (bit 07 RKCS1) of the currently selected RK unit.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	ATN 3	ATN 2	ATN 1	ATN 0	0	0	0	0	0	0	0	0

Figure 11-8 Attention Summary Register (RKAS)

RKAS<08-11> - Attention (ATT)

One of these 4 bits will be set according to the drive select bits in RKCS2 when the ready bit is set in RKCS1.

DESIRED CYLINDER REGISTER (RKDC)

The RKDC register (Figure 11-9) can be read or written via program control and is used to store the address of the desired cylinder. Following an initial load, the value in the RKDC register will be

incremented by one whenever the track address (TA0-TA2) value in the RKDA register overflows during a data transfer. When the RKDC register is incremented and the RKWC register is not equal to zero, a single-cylinder seek is initiated by the controller.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	DC 9	DC 8	DC 7	DC 6	DC 5	DC 4	DC 3	DC 2	DC 1	DC 0

Figure 11-9 Desired Cylinder Register (RKDC)

RKDC<00-09> -Desired Cylinder (DC0-DC9)

For an H disk drive, valid cylinder addresses range from the outer edge of the disk (0) to the centre (252 decimal), requiring eight (DC0-DC7) address bits to define the range (000-374 octal).

For a G disk drive, valid cylinder addresses range from the outer edge of the disk (0) to the centre (874 decimal), requiring ten (DC0-DC9) address bits to define the range (0000-1552 octal).

For a J disk drive, valid cylinder addresses range from the outer edge of the disk (0) to the centre (979 decimal), requiring ten (DC0-DC9) address bits to define the range (0000-1723 octal).

For a K disk drive, valid cylinder addresses range from the outer edge of the disk (0) to the centre (839 decimal), requiring ten (DC0-DC9) address bits to define the range (0000-1507 octal).

BUS ADDRESS EXTENSION REGISTER (RKBAX)

For systems with parity memory, this register (Figure 11-10) contains the memory address extension bits, which in conjunction with the low order address bits from RKBA form a 24 bit starting address for disk transfers.

15								07	06	05	04	03	02	01	00
								BA 23	BA 22	BA 21	BA 20	BA 19	BA 18	BA 17	BA 16

Figure 11-10 Bus Address Extension Register (RKBAX)

TYPE REGISTER (RKTYP)

This read only register provides status information about the drive size and type, and the mapping mode as selected by the switches on the T-Board.

All zeros in this register indicate an H or G system.

If bit 7 (RKTYP) is set then RKTYP bits 00 and 01 have the following significance:

RKTYP		
Bit 01	Bit 00	Meaning
0	0	K, RK07 mapping
0	1	J, RK07 mapping
1	0	K, Native mapping
1	1	J, Native mapping

11.2 DISK COMMANDS

Disk commands are divided into two groups. One group (non-data handling) is concerned with the various operational requirements of the drive, while the second group (data or header handling) is concerned with the transfer of data or header information to or from the drive. (Refer to Table 11-2).

The controller recognizes a command by the configuration of the 4-bit command code (F4-F1) that is loaded into RKCS1. However, the command will not be decoded for execution until bit position zero (GO) of the register is set. In addition, two other RKCS1 bit positions are significant to command flow: The Ready (RDY) bit (bit 7) is set when the execution of a command is completed and the combination Error/Clear (CERR/CCLR) bit (bit 15) will be set if a drive or controller error occurs during execution. With these considerations, the disk commands can initiate the operations shown in the table.

Table 11-2 Disk Commands

Command	Function Code F4	F3	F2	F1	G0	Octal
Non-data Handling						
Select Drive	0	0	0	0	1	01
Set Status	0	0	0	1	1	03
Drive Clear	0	0	1	0	1	05
Unload	0	0	1	1	1	07
Start Spindle	0	1	0	0	1	11
Recalibrate	0	1	0	1	1	13
Seek	0	1	1	1	1	17
Data or Header Handling						
Read Data	1	0	0	0	1	21
Write Data	1	0	0	1	1	23
Write Header	1	0	1	1	1	27
Write Check	1	1	0	0	1	31
Read Format	1	1	1	0	1	35

Select Drive (01)

This command is used to obtain the return of drive status information.

Set Status (03)

This command is the same as the Select Drive command.

Drive Clear (05)

This command is used to clear all error flags in the selected drive, provided the error(s) themselves are no longer present.

Unload (07)

This command is used to unload the heads in the drive and stop the spindle.

Start Spindle (11)

This command is used to start the spindle and load the heads in the drive.

Recalibrate (13)

This command is used to relocate the heads to cylinder zero (address of the outermost cylinder on the disk) and to clear the drive's Cylinder Address register.

Seek (17)

This command directs the drive to relocate the heads over a new cylinder. The new cylinder address is derived from the Desired Cylinder register (RKDC). When the seek is completed, the CDA bit is set in RKDS.

Read Data (21)

The following sequence is executed entirely by the controller. A Seek to the cylinder in RKDC is performed. When the READY signal from the drive becomes true, headers are read and compared with the desired disk address until the correct sector is found. Transfer of data through the Silo data buffer to memory is initiated. When the sector data transfer is complete and assuming there are no data errors, the word count in RKWC is checked. If non-zero, the data transfer operation is repeated into the next sector. The word count is checked at the end of each sector until it reaches zero, at which time the command is terminated by setting the READY bit.

Write Data (23)

The following sequence is executed entirely by the controller. A Seek to the cylinder in RKDC is performed. When the READY signal from the drive becomes true, headers are read and compared with the desired disk address until the correct sector is found. Preamble, Data (256 words) and CRC bits (16) are written on the disk. If the word count in RKWC goes to zero during the sector, the rest of the sector is zero-filled. After the sector transfer, the word count in RKWC is checked and if non-zero, the data transfer operation is continued into the next sector. The word count in RKWC is checked at the end of each sector and when it equals zero, the command is terminated by setting the READY bit.

Write Header (27)

The following sequence is executed. A Seek to the cylinder in RKDC is performed. When the READY signal from the drive becomes true, the controller then waits for INDEX from the drive and then waits for the first sector pulse. Then the header preamble, including sync 1 and the three header words are written. The all-zero gap, the data preamble (including sync 1) and all-zero data, CRC, postamble and the end-of-sector gap are written. This is repeated in each successive sector until Index is encountered again and the command is terminated. The READY bit is then set.

NOTE:

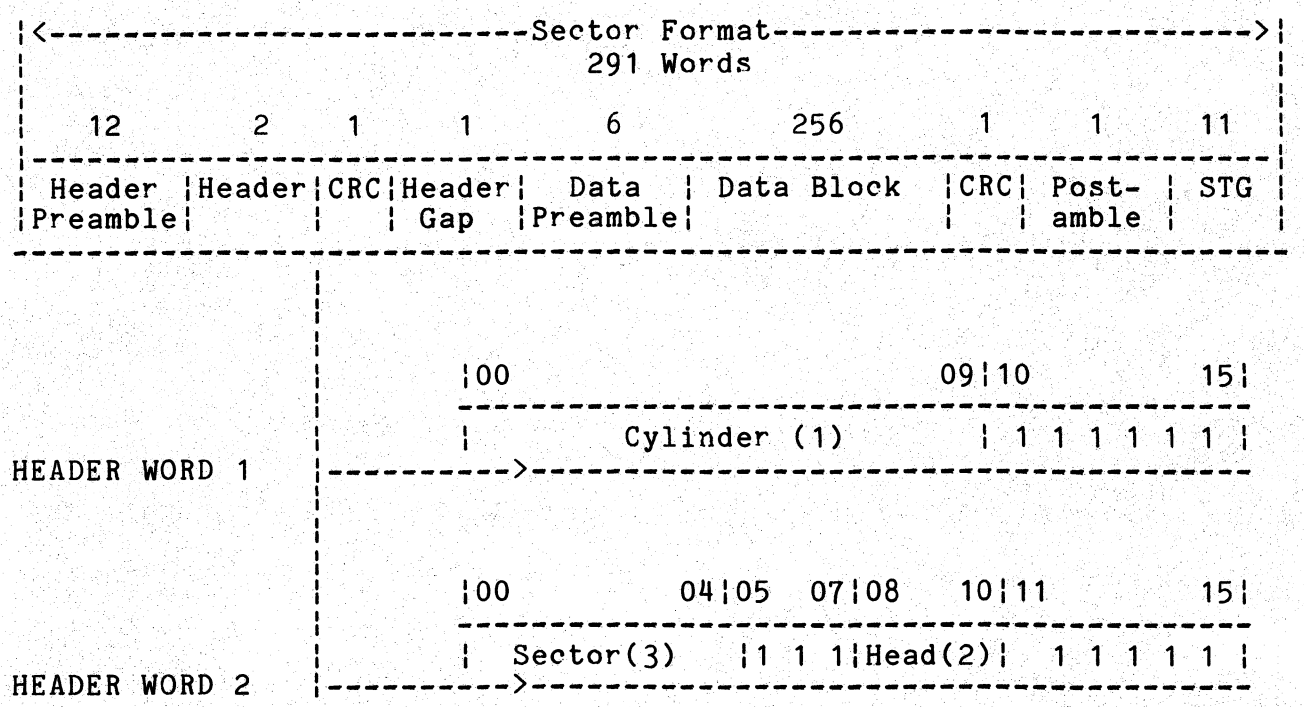
The 2 words of the header (Desired Cylinder and Disk Address) are prepared by software and treated as data by the controller. The controller then appends a CRC word. (Figure 11-11). Only one complete track can be formatted at a time. Either 22 or 23 headers will be written depending on the word count. RKWC must be set to -66 or -69 decimal.

Write Check (31)

The following sequence is executed entirely by the controller. A Seek to the cylinder in RKDC command is performed. When the READY signal from the drive becomes true, the drive provides data as in a Read command and data is obtained from memory as in a Write command. The data are compared on a word for word basis until the word count reaches zero or until a failure to compare occurs. If the data fails to compare, the command is immediately terminated.

Read Format (35)

The following sequence is executed. A Seek to the cylinder in RKDC is performed. When the READY signal from the drive becomes true, the controller waits for Index from the drive and then waits for the first sector pulse. The 2 sector header words are read by the controller and are transferred via the Silo buffer into main memory. This is repeated for the remaining 22 sectors after which the command is terminated and the READY bit is set.



Coding

STG	Sector Tolerance Gap		
(1)	Cylinder	1s complement	(000-374 octal) for model H
			(0000-1552 octal) for model G
			(0000-1723 octal) for model J
			(0000-1507 octal) for model K
(2)	Track	1s complement	(head 0, 1, 2)
(3)	Sector	1s complement	(00-25 octal)

Figure 11-11 Sector Formats

11.3 ERROR DETECTION AND CORRECTION

When a write data command (Write) is executed, a 16-bit Cyclic Redundancy Code (CRC) is generated by the data and, following the recording of the data field, is written in the CRC field. When a read data command (Read, Write Check) is executed, the CRC field is also read to verify the integrity of the recorded data. If a read error is detected, the read function of the current command is disabled and the following indicators are set:

Error Correction Hard (ECH) bit (bit 6 in RKER);

Data Check (DCK) error bit (bit 15 in RKER);

Controller Error (CERR) bit (bit 15 in RKCS1);

Ready (RDY) bit (bit 7 in RKCS1).

When a data error is indicated (ECH, DCK, CERR), the program must initiate a data recovery routine to provide a sequence of 16 successive rereads.

Any one of the 16 rereads could result in the recovery of data. Typically this could occur if an error-producing material (eg., dirt specks) either disappeared from that area of the disk surface or diminished to a point that allowed the data to become readable.

It should be understood that for every required reread cycle, the Disk Address (DA) register must be reloaded and the GO bit (0) in RKCS1 reasserted. Thus a disk revolution is lost every time a reread cycle is executed.

11.4 PROGRAMMING EXAMPLES

The following material provides several examples of H (RK06) subsystem programming. The G, J and K subsystems (RK07) programming is approached in a similar manner.

RK06 Device Driver Routine

The RK06 Device Driver routine allows a user to establish communications with a device and determine subsystem status and availability.

```
,TITLE RK06 DEVICE DRIVER

;CALLING SEQUENCE
;    JSR  PC,RK06
;    DRIVE UNAVAILABLE RETURN
;    NORMAL RETURN
;
;INPUTS:
;    UNIT = DESIRED UNIT NUMBER IN BITS 0-2
;    DSKADR = TRACK/SECTOR ADDRESS
;    BUSADR = LOW ORDER 16 BITS OF Q-BUS ADDRESS
;    WCNT = TWO'S COMPLEMENT WORD COUNT
;    CYLADR = DESIRED CYLINDER ADDRESS
;    FUNCTN = DESIRED FUNCTION + IE + A16-A17
```


```
            ;
            ;OUTPUTS:
            ;    RK6ACT SET IF RK06 IS ACTIVE
            ;-
      RKCS1=     177440     ;RKCS1 (base Q-Bus address)
      RKCS2=     RKCS1+10   ;RKCS2
      RKDS=      12         ;RKDS offset from RKCS1
      RKER=      14         ;RKER offset from RKCS1
      RKDC=      20         ;RKDC offset from RKCS1
      SELDRV=    1          ;Basic Select Drive function
      SCLR=      40         ;Subsystem Clear
      SVAL=      100000     ;Status Valid
      DRDY=      000200     ;Drive Ready
      DRA=       000001     ;Drive Available
      UNS=       040000     ;Drive Unsafe
      CERR=      100000     ;Controller Error/Controller Clear
      DI=        040000     ;Drive Interrupt
      IE=        000100     ;Interrupt Enable

UNIT:       .WORD 0          ;Desired unit # in bits 0-2
DSKADR:     .WORD 0          ;Track/sector address
BUSADR:     .WORD 0          ;Low order 16 bits of Q-bus address
WCNT:       .WORD 0          ;Two's complement word count
CYLADR:     .WORD 0          ;Desired cylinder address
FUNCTN:     .WORD 0          ;Desired function + IE + A16-A17 + GO
RK6ACT:     .BYTE 0          ;1-if RK06 currently active
POSPRO:     .BYTE 0          ;1-if doing Seek/Recal function

RK06: TSTB    RK6ACT                ;Is the RK06 currently active?
      BNE     RK06                  ;Wait for it to become active
      MOV     #RKCS2,R2             ;Point to CS2 register
      MOV     #SCLR,(R2)            ;Issue a Subsystem Clear
      MOV     UNIT,(R2)             ;Select the desired unit
      MOV     DSKADR,-(R2)          ;Load RKDA
      MOV     BUSADR,-(R2)          ;Load RKBA
      MOV     WCNT,-(R2)            ;Load RKWC
      MOV     #SELDRV,-(R2)         ;Issue drive select
1$:   TSTB    (R2)                  ;
      BPL     1$                    ;Wait ready
      MOV     RKDS(R2),R1           ;Get Drive Status register
      COM     R1                    ;Complement bits
      BIT     #SVAL!DRDY!DRA,R1     ;Can drive accept further
                                     commands?
      BNE     4$                    ;If NE no
      BIT     #UNS,RKER(R2)         ;Is this a Seek function?
      BNE     4$                    ;If NE yes
      MOV     CYLADR,RKDC(R2)       ;Load cylinder address
      INCB    POSPRO                ;Indicate positioning command
      ADD     #2,(SP)               ;Show a good return
      INCB    RK6ACT                ;Set RK06 active flag
      MOV     FUNCTN,(R2)           ;Load RKCS1
4$:   RTS     PC                    ;Return to users program
```


```
;INTERRUPT SERVICE ROUTINE

INTR:  MOV     #RKCS1,R2           ;Point to CS1 register
       TSTB    POSPRO              ;Positioning in progress?
       BEQ     5$                  ;If EQ no
       BIT     #CERR!DI,(R2)       ;Positioning complete or error?
       BNE     5$                  ;If NE yes
       RTI                         ;Wait for positioning to complete

5$:    BIC     #CER!IE,(R2)        ;Clear IE without doing a CCLR
       CLRB    POSPRO              ;Reset positioning in progress
       TST     (R2)                ;Any errors?
       BMI     20$                 ;Yes, process directly
       TST     RKDS(R2)            ;Is current status valid?
       BMI     20$                 ;Yes it is
       MOV     #SELDRV,(R2)        ;Select drive to get fresh status
10$:   TSTB    (R@)                ;
       BPL     10$                 ;Wait ready
20$:   TST     (R2)                ;Any errors?
       BPL     40$                 ;If PL no
;+
;
;
;The user now handles any error conditions
;
;
;-
40$:   CLRB    RK6ACT              ;Set RK06 inactive
       RTI                         ;Return to user

       .END
```

11.5 PROGRAMMING CONSIDERATIONS

The following provides a selection of pertinent programming considerations.

Flagging a Bad Sector

Since a Write Header command cannot be used to selectively write individual sectors, an entire track is written when the command is executed. Therefore, if a programmer desires to flag a bad sector, all currently recorded sector and data information from the desired track must be extracted and preserved elsewhere for rewriting along with the new information.

Unit Selection

When the Controller Clear (CCLR) bit (bit 15 in RKCS1) is asserted (via the Q-bus), the Drive Select (DS0-DS1) bits (bits 00,01 in RKCS2) are cleared. Therefore, before the next command is initiated, unit selection must be reconfigured.

Enabling an Interrupt

The Interrupt Enable (IE) bit (Bit 6 in RKCS1) must be set prior to the initiation of an operation or an interrupt will not be generated.

Drive Ready Requirement

A Seek, or any other head motion command, will be ignored by a drive if the Drive Ready (DRDY) bit is not asserted in the RKDS register when the command is initiated.

INTRODUCTION

The magnetic tape subsystem performs eight functions. A function is initiated by a GO command after the processor has issued a series of instructions that store function-control information into controller registers. To accept a command and perform a function, the controller must be properly addressed and the tape drives must be powered up at operational speed and be ready.

All software interaction between the tape controller, the processor and processor memory, is accomplished by six registers in the tape controller. These registers are assigned memory addresses and can be read or written into (except where noted) by instructions that reference respective register addresses.

12.1 DEVICE REGISTERS

STATUS REGISTER (MTS)

The Status register (Figure 12-1) is a read only register.

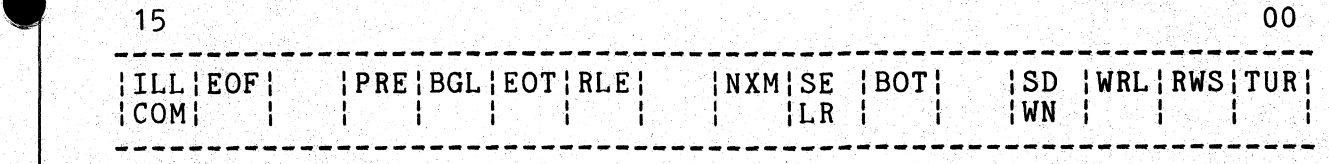


Figure 12-1 - Status Register (MTS)

MTS<00> - Tape Unit Ready (TUR)

Set when the selected tape unit is stopped and when the Select Remote (Bit 6) is false. Cleared when the processor sets the GO bit and the operation defined by the function bit occurs.

MTS<01> - Rewind Status (RWS)

Set by the master as soon as it receives a rewind command from the control unit. Cleared by the master as soon as the tape arrives at the BOT (Bit 5) marker in the forward direction. (It overshoots BOT in the reverse direction).

MTS<02> - Write Lock (WRL)

Set to prevent the control unit from writing information on tape. Controlled by presence or absence of the write protect ring on the tape reel.

MTS<03> - Tape Settle Down (SDWN)

Set whenever the tape unit is slowing down. The master will accept and execute any new command during the SDWN period except if the new command is to the same tape unit as the one issuing SDWN and if the direction implied in the new command is opposite to the present direction.

MTS<05> - Beginning of Tape (BOT)

Set when the BOT marker is read and cleared when the BOT marker is not read. BOT at a 1 does not produce a 1 in the ERR bit.

MTS<06> - Select Remote (SELR)

Cleared when the tape unit addressed does not exist, is offline or is powered off.

MTS<07> - Non-existent Memory (NXM)

Set during NPR (Non-processor Request) operations when the control unit is bus master, is performing data transfers into and out of the bus and when the control unit does not receive an RPLY signal within 10 microseconds after it has issued a DIN or DOUT signal. The operations which occur when the error is detected are identical to those indicated for the BGL (Bit 11) error.

MTS<09> - Record Length Error (RLE)

Detected only during a read operation. It occurs for long records only and is indicated as soon as MTBRC increments beyond 0; at which time both data transfer into memory and incrementing of the MTCMA and MTBRC stop. However, the control unit reads the entire record and sets the ERR bit when the LPC character is read. CU ready (Bit 7 of MTC) remains at 0 until the LPC character is set.

MTS<10> - End of Tape (EOT)

Set when the EOT marker is read while the tape is moving in the forward direction. The bit is cleared as soon as the same point is read while the tape is moving in the reverse direction. The ERR (Bit 15 of MTC), as a result of the EOT bit at a 1, sets only in the tape forward direction and coincidentally with the reading of an LPC (longitudinal parity check) character.

MTS<11> - Bus Grant Late (BGL)

Set when the control unit, after issuing a request for the bus, does not receive a bus grant before the controller receives the bus request for the following tape character. The condition is tested only for NPR operations. The ERR bit sets simultaneously with BGL, thus terminating the operation. If the BGL occurred during a write or write with extended IRG operation, the control unit does not send the signal WDS to the master and the master writes the CRC (if required) and LPC characters onto the tape, terminating the record.

MTS<12> - Hard Error (HE)

Set as the result of an error being detected on tape.

For all errors, the ERR bit sets at the end of the record. Both lateral and longitudinal parity errors are detected during a read, write, write EOF and write with extended IRG operations. The entire record is checked including the CRC and LOC characters. During a write operation a correctable error in the PE (1600 bpi) mode will set this bit.

MTS<14> - End of File (EOF)

Set when an EOF character is detected during a read, space forward or space reverse operation. During the read or space forward operation, the EOF bit is set when the LPC character following the EOF character is read. During a space reverse operation, the EOF bit is set when the EOF character following its LPC character is read. The ERR bit sets when the LPC character strobe is generated with the File Mark signal, on EOF detection.

MTS<15> - Illegal Command (ILL COM)

Set by any of the following illegal commands:

Any DATO or DATOB to the command register during the tape operation period;

A write, write EOF, or write with extended IRG operation, when the File Protect bit is 1;

A command to a tape unit where SELR (Bit 6) is 0;

SELR (Bit 6) becoming a 0 during an operation.

In the first three error conditions listed, the command is loaded into the MTC but the GO pulse to the tape unit is not generated. In addition, the CU ready bit remains set.

COMMAND REGISTER (MTC)

The functions of the bits of the Command Register (Figure 12-2) are as follows -

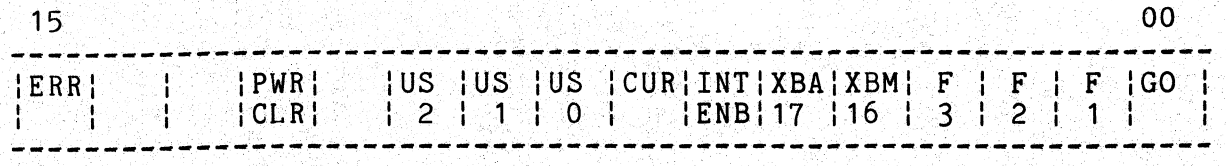


Figure 12-2 - Command Register (MTC)

MTC<00> - Go (GO)

When set, begins the operation defined by the function bits.

MTC<01-03> -Function Codes (F1-F3)

Selects one of 8 functions (programmable commands) with the setting of the GO bit:

Command	F3	F2	F1	GO	Octal
Off Line	0	0	0	1	01
Read	0	0	1	1	03
Write	0	1	0	1	05
Write EOF	0	1	1	1	07
Space Forward	1	0	0	1	11
Space Reverse	1	0	1	1	13
Write with Extended Inter-record Gap	1	1	0	1	15
Rewind	1	1	1	1	17

MTC<04-05> - Address Bits (XBA,XBM)

Extended memory bits for an 18-bit bus address. Bit 5 corresponds to XBA17 and Bit 4 to XBA16. They are an extension of the MTCMA and increment during a tape operation if there is a carry out of MTCMA.

MTC<06> - Interrupt Enable (INT ENB)

When set, an interrupt occurs whenever either the CU ready bit or the ERR bit change from 0 to 1, or, whenever a tape unit that was set into rewind has arrived at the beginning of tape. In addition, an interrupt occurs on an instruction that changes the INT ENB from 0 to 1 and does not set the GO bit, ie., CU READY or ERROR = 1.

MTC<07> - CU Ready (CUR)

Cleared at start of a tape operation and set at end of tape operation. The control unit accepts as legal, all commands it receives while the CU Ready bit is 1.

MTC<08-09> - Unit Select 1 (US1)

Specifies one of the four possible magnetic tape units. All operations defined in the MTC and all status conditions defined in the MTS, pertain to the unit indicated by these bits. Cleared on INIT.

MTC<10> - Unit Select 2 (US2)

Selects high-speed streaming mode.

MTC<12> - Power Clear (PLCR)

Provides the means for the processor to clear the control unit and tape units without clearing any other device in the system. The processor always reads back the PCLR bit as 0.

MTC<15> - Error (ERR)

Set as a function of bits 7-15 of the Status Register (MTS). Cleared by INIT or on the GO command to the tape unit.

BYTE RECORD COUNTER REGISTER (MTBRC)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Figure 12-3 - Byte Record Counter Register (MTBRC)

The MTBRC (Figure 12-3) is a 16-bit binary counter which is used to count bytes in a read, write, write with extended IRG operation, or records in a space forward or space reverse operation. When used in a write or write with extended IRG operation, the MTBRC is initially set by the program to the 2's complement of the number of bytes to be written on tape. The MTBRC becomes 0 after the last byte of the record has been read from memory. Thus, when the next WDS (Write Data Strobe) signal occurs from the master, the control unit will not send the WDR (Write Data Request) to the master, indicating that there are no more data characters in the record.

When the MTBRC is used in a read operation, it is set to a number equal or greater than the 2's complement of the number of bytes to be loaded into memory. A record length error (RLE) occurs for long records only and is indicated when a read pulse for data (RDS occurring when CRCS or LPCS does not occur) occurs when the MTBRC is 0. The MTBRC increments by 1 immediately after each memory access.

When the MTBRC is used in a space forward or space reverse operation, it is set to the 2's complement of the number of records to be spaced. It is incremented by a 1 at LPC time, whether the tape is moving in the forward or reverse direction. A new GO pulse is sent to the tape unit during the SDWN time if the MTBRC is not 0 during that time. When the tape unit is moving in reverse, the LPC character is detected before SDWN but before the entire record has been traversed. Thus, both SWDN and LPC characters appear to be in different positions on tape from those when the tape unit is moving forward.

CURRENT MEMORY ADDRESS REGISTER (MTCMA)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Figure 12-4 - Current Memory Address Register (MTCMA)

The MTCMA (Figure 12-4) contains 16 of the possible 18 memory address bits. It is used in NPR operations to provide the memory address for data transfers in read, write and write with extended IRG operations. Prior to issuing a command, the MTCMA is set to the memory address into which the first byte is loaded in a read operation, or from which the first byte is read in a write or write extended IRG operation. The MTCMA is incremented by 2 immediately after each memory access. thus, at any point in time, the MTCMA points to the next higher address than the one which has most recently been accessed. When the entire record has been transferred, the MTCMA contains the address plus 2 of the last characters in the record. In the error conditions Bus Grant Late (BGL) and Non-existent Memory (NXM), the MTCMA contains the address of the location in which the failure occurred.

The MTCMA is available to the processor on a DATI except bit 0 which always reads as zero under program control. Bit 0 can be asserted during NRPs to determine the selected byte. The bits are set or cleared on a processor DATO. INIT clears all bits in the MTCMA.

DATA BUFFER REGISTER (MTD)

15															00
							DB 08	DB 07	DB 06	DB 05	DB 04	DB 03	DB 02	DB 01	DB 00

Figure 12-5 - Data Buffer (MTD)

The Data Buffer (Figure 12-5) is a 9-bit register which is used during a read, write, or write with extended IRG operation. In a read operation, the data buffer is a temporary storage register for characters read from tape before being stored into memory. In a processor read, all nine bits are stored into memory. Bits 0-7 in memory correspond to channels 7 through 0 respectively from tape and bit 8 corresponds to the parity bit. In a DMA operation, only the data bits are read into memory and are alternately stored into the low and high bytes. In a write or write with extended IRG operation, the data buffer is a temporary storage register for characters read from core memory before they are written on tape.

In a read operation, the LPC character enters the data buffer when bit 14 of MTRD is 1 and is inhibited from doing so when bit 14 is 0. Thus, after reading a nine-channel tape, the data buffer contains the LPC character when bit 14 is 1 and the CRC character when bit 14 is 0. After reading an EOF character, the data buffer contains all 0's when bit 14 is a 1 and the LPC character when bit 14 is 0. The MTD is available to the processor on a DATI. Bits 9 through 15 are read identically to bits 1 through 7 respectively. Bits 0 through 7 are set or cleared on a processor DATO. Bits 8 through 15 are not affected by a processor DATO. INIT clears all bits in the MTD.

TAPE READ LINES REGISTER (MTRD)

Refer Figure 12-6 for the memory locations allocated for the tape read lines.

15															00
TIMER	CRC/ LPC		GS				P	CH 0	CH 1	CH 2	CH 3	CH 4	CH 5	CH 6	CH 7

Figure 12-6 - Tape Read Lines Register (MTRD)

MTRD<00-07>

Channels (CH7-0)

MTRD<08>

Parity bit (P)

MTRD<12>

Gap Shutdown bit (GS)

MTRD<14>

CRC or LPC character selector (CRC/LPC)

MTRD<15> - Timer

TIMER is a 10 kHz signal with a 50% duty cycle. The signal is used for diagnostic purposes in measuring the time duration of the tape operations.

For correct longitudinal parity, MTRD 0-8 are 0 after writing a record or reading a record from tape. For a longitudinal parity error, one or more of the bits 0-8 remains at 1. The bits are at a 1 indicating the channel(s) containing the error which sets the CU ready bit. Thus, if the pulse is set during a tape operation, CU ready sets prematurely thus producing the gap shutdown period when characters are still being read. MTRD 0-8 are set and cleared by the tape unit. MTRD 14 is set and cleared by the processor and cleared by INIT. MTRD 15 is uniquely controlled by the 100 microsecond timer. The MTRD is available to the processor on a DATO except that bit 13 reads back as a zero.

INTRODUCTION

Parity memory modules (X-Board), are MOS, random access memories, designed to be used in conjunction with the GPMI-Y controller. This two-board set is used in place of the GPMI-S controller for all SS23 Spectrum models where memory exceeds 256 kilobytes.

Each parity memory module contains parity control circuitry and a control and status register.

CONTROL AND STATUS REGISTER (CSR)

The Control and Status register allows program control of certain parity functions, and contains diagnostic information if a parity error has occurred. The CSR register (Figure 14-1) contains bits that are used to store the parity error address. By setting a bit in the CSR, wrong parity can be forced. This diagnostic tool is useful for checking out the parity logic. The CSR has its own address in the top 8 kilobytes of memory and can be accessed by a bus master via the Q-bus. All CSR bits are cleared by assertion of BUS INIT L

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PE	RE EN			A17	A16 or A23	A15 or A22	A14 or A21	A13 or A20	A12 or A19	A11 or A18			WR		ERR EN

Figure 14-1 Control and Status Register (CSR)

CSR<00> - Parity Error Enable (ERR EN)

If set, and a parity error occurs on a DATI or DATIO(B) cycle to memory, then BDAL 16(L) and BDAL 17(L) are asserted on the bus at the same time as the data. This bit is read/write and is reset to zero on power-up or BUS INIT.

CSR<02> - Write Wrong Parity (WR)

When set, this bit causes wrong parity to be written into memory for every subsequent memory write operation. This bit may be used to check the parity error logic as well as failed address information in the CSR. The following diagnostic is applicable:

With bit 02 set, write entire memory with any pattern.

Read first location in memory. If bit 0 of the CSR is set, then a parity error should be detected on the Q-Bus and the failed address at location (0) is stored in the CSR.

Read the CSR and obtain the failed address. If CSR bit 14 equals 0, then bits A11-A17 are loaded into CSR bits 05-11. If CSR bit 14 equals 1, then bits A18-A23 have been loaded into CSR bits 05-10. Bit 02 is a read/write bit reset to zero on power-up or BUS INIT.

CSR<05-11> - Error Address Bits (A11-A23)

If a parity error occurs on a DATI or DATIO(B) cycle, then A11-A17 are stored in CSR bits 05-11 and bits A18-A23 are latched. The CSR bit 14 set to 0 allows the logic to pass A11-A17 to the Q-Bus. A 22-bit machine requires two reads. The first read (with CSR bit 14 set to 0) enables A11-A17 to be read from CSR bits 05-11. Then the software must set CSR bit 14 equal to 1 to enable A18-A23 to be read from CSR bits 05-10.

The parity error address locates a parity error to a 2 kilobyte segment of memory. These are read only bits and are reset to zero via power-up or BUS INIT. If a second parity error is found, the new failed address will be stored in the CSR.

CSR<14> - Extended CSR Read Enable (RE EN)

Refer to the Error Address bits paragraph for a description of this bit's function.

CSR<15> - Parity Error (PE)

When set, this bit indicates that a parity error has occurred. Bit 15 is a read/write bit. It is reset to zero via power-up or by BUS INIT and will remain set unless rewritten or initialized.

INTRODUCTION

The SPECTRUM ELEVEN bootstrap listings are both detailed in this chapter.

The first listing is for all Spectrum models using the GPMI-S controller; the second listing applies to models using the GPMI-Y controller in conjunction with the X-Board parity memory module.

BOOTSTRAP LISTING 1

```
.c;@^BOOTSTRAP LISTING 1^@


                        ;
                        ;Initialization.
                        ;
                        .IF DF, $LIST$
000000                  .ASECT
        173000          .=173000                ;For listing purposes only
                                                ;Code is completely relocatable
                        .ENDC
                        ;
173000                  BOOT::;
173000  000005          RESET                   ;Reset everything in case
                                                ;we were started from the
                                                ;console (via micro-ODT)
173002  012706          MOV     #1000,SP        ;Stack

                        ;
173006  012703          MOV     #ITSIZE,R3      ;Iterator size register

173012  012704          MOV     #ITFUNC,R4      ;Function (and, Read Only

                                                ;memory size)
173016  012705          MOV     #ITCSR,R5       ;Control and Status
```


```
MEMORY TEST ROUTINE
173022          MEMTEST:
173022  012737          MOV     #-1,@#ITSADD    ;Memory set data


                ;
                ;
173030  010702          MOV     PC,R2
173032  000465          BR      ITGO            ;Set 0-128Kb to -1
                ;
                ;
173034  010702          MOV     PC,R2
173036  000463          BR      ITGO            ;Set 128-256Kb to -1
                ;
                ;All memory set to -1. (If memory is <  256Kb
                ;iterator will wrap around. This does not matter.)
                ;
                ;Commence Well Test. This is done in 32Kb blocks,
                ;because the memory size, in ITFUNC, is given in
                ;number of 32Kb blocks.
                ;
173040  011400          MOV     (R4),R0         ;Get size of memory
                                                ;in 32Kb blocks
                ;
173042  005037          CLR     @#ITDEXT        ;First block of memory

173046  012715          MOV     #ITC$MF,(R5)    ;Indicate to Iterator
                                                ;That Well test wanted
173052  012713  10$:    MOV     #140000,(R3)    ;32Kb to be tested.

                ;
                ;
173056  010702          MOV     PC,R2
173060  000452          BR      ITGO            ;Check it (?MEM error
                                                ; if failure detected)
173062  077005          SOB     R0,10$          ;All Memory Tested?
                                                ;Yes
                ;
173064  004767          JSR     PC,INTRAP       ;Set up trap vectors
```


```
                        ;
173070  012704  DMLOAD: MOV     #WCS1,CSR       ;Set up CSR address
                        ;
173074  012702         MOV     #100200,R2      ; end test for later
                        ;
173100  012714         MOV     #1,(CSR)        ;Select the drive
173104  103473         BCS     SFLOAD          ;No Winchester Controller
                        ;
173106  030214  10$:    BIT     R2,(CSR)        ;Select finished?
173110  001776         BEQ     10$             ;No - wait
                        ;
173112  005001         CLR     R1              ;Assume drive type is RK06
                        ;
173114  032737         BIT     #400,@#WDS      ;Drive RK06 or RK07?
173122  001402         BEQ     20$             ;RK06
                        ;
173124  012701         MOV     #2000,R1        ;Set type to RK07
                        ;
173130  012700  20$:    MOV     #100011,R0
173134  050100         BIS     R1,R0           ;Include drive type
173136  010014         MOV     R0,(CSR)        ;Issue command
                        ;
173140  030214  30$:    BIT     R2,(CSR)        ;Finished yet?
173142  001776         BEQ     30$             ;No - wait
173144  100413         BMI     DMLERR          ;Error - may be offline
                        ;
173146  012737         MOV     #-256.,@#WWC    ;1 Block transfer
173154  012700         MOV     #21,R0          ;Command: <READ> <GO>
173160  050100         BIS     R1,R0           ;Include Drive type
173162  010014         MOV     R0,(CSR)        ;Issue command
                        ;
173164  030214  40$:    BIT     R2,(CSR)        ;Primary Boot Read in yet?
173166  001776         BEQ     40$             ;No - wait
173170  100401         BMI     DMLERR          ;In Error
                        ;
173172  005007         CLR     PC              ;jump to code just read in.
                        ;
173174  032737  DMLERR: BIT     #10000,@#WCS2   ;Winchester Off-line?
173202  001034         BNE     SFLOAD          ;Yes
                        ;
173204                 MESSAGE DM              ;No - Error Message
```


```
                        ;
                        ;Start Iterator and wait for it to finish
                        ;
173206  012714  ITGO:   MOV     #ITF$MT,(R4)    ;Say 'GO'

                        ;
173212  105715  10$:    TSTB    (R5)            ;Finished Yet?
173214  100376          BPL     10$             ;No
                        ;
173216  005713          TST     (R3)    ;Any errors found?
                                        ;(if there were, ITSIZE would be
                                        ;non zero, which when added to
                                        ;ITDADD & ITDEXT points at the
                                        ;word in error.
                                        ;
173220  001002          BNE     MER     ;Error found. Very non-structured
                                        ;but anything goes in a Bootstrap.
                                        ;
173222  000162          JMP     2(R2)

                        ;
                        ;Memory Test Failure
                        ;
173226  004767  MER:    JSR     PC,INTRAP       ;Initialize TRAP vectors

173232                  MESSAGE MEM
                        ;
                        ;Set up TRAP vectors
                        ;
173234  010701  INTRAP: MOV     PC,R1           ;Set up trap vectors
173236  062701          ADD     #<T4ADDRR-.>,R1

173242  012702          MOV     #4,R2           ;4 - Time out etc

173246  010122          MOV     R1,(R2)+        ;Trap pointer
173250  012712          MOV     #340,(R2)       ;And processor status

                        ;
173254  062701          ADD     #<TRPADD-T4ADDR>,R1

173260  012702          MOV     #34,R2          ;Trap instruction vector

173264  010122          MOV     R1,(R2)+        ;Vector address
173266  012712          MOV     #340,(R2)       ;And processor status

173272  000207          RTS     PC
```


SF (FLOPPY) DISK BOOTSTRAP

```
                        ;
                        ;Set up Registers
                        ;
173274                  SFLOAD:
173274  012701                  MOV     #-1,ONES

173300  012705                  MOV     #SFSECT,SECT

173304  005015                  CLR     (SECT)  ;Note that this instruction must be
                                                ;here, because the floppy disk
                                                ;controller chip, which this register
                                                ;is in, needs some time to repond.
                                                ;Therefore if CLR was immediately
                                                ;followed by the TST (below) the
                                                ;chip may not have time to repond
                                                ;correctly.
173306  012702                  MOV     #SFSEL,SEL

173312  012703                  MOV     #SFCTRL,CTRL

173316  012704                  MOV     #SFCSR,CSR

                        ;
173322  005715                  TST     (SECT)          ;Controller present?
173324  001050                  BNE     MTLOAD          ;No - try the MT
                        ;
                        ; Wiggle all head motors to ensure track centering
                        ;
173326  010012          WIGGLE: MOV     R0,(SEL)        ;Select Drive
173330  012714                  MOV     #276,(CSR)              ;Step In

                        ;
173334  105713                  TSTB    (CTRL)          ;Finished?
173336  100376                  BPL     .-2             ;No - wait
                        ;
173340  012714                  MOV     #236,(CSR)      ;Step out

                        ;
173344  105713                  TSTB    (CTRL)          ;Finished?
173346  100376                  BPL     .-2             ;No - wait
                        ;
173350  005200                  INC     R0              ;Next drive
173352  042700                  BIC     #177774,R0      ;Back to drive zero?

173356  001363                  BNE     WIGGLE          ;No - wiggle this drive
                        ;
173360  052700                  BIS     #10,R0          ;Set double density bit.

                        ;
                        ;Now search for the first on-line drive
                        ;
173364                  DSEARCH:
173364  010012                  MOV     R0,(SEL)        ;Select drive
173366  105714                  TSTB    (CSR)           ;On-line?
173370  100405                  BMI     10$             ;Yes
                        ;
```

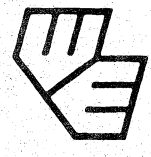

```
9       173372  005200          INC     R0              ;Select next drive
173374  032700          BIT     #4,R0           ;There can only be 4 drives

173400  001771          BEQ     DSEARCH         ;OK!
                ;
173402  000421          BR      MTLOAD          ;No SF floppies on line. Boot
                                                ;off the MT (if there is one)
                ;
                ;Boot off the on-line drive
                ;
173404  012714  10$:    MOV     #376,(CSR)      ;Home Seek

                ;
173410  105713          TSTB    (CTRL)          ;Finished?
173412  100376          BPL     .-2             ;No - wait
                ;
173414  012737          MOV     #-512.,@#SFSIZE ;512 byte transfer


                                                ;address zero
                ;
173422  010137          MOV     ONES,@#SFSECT   ;From sector zero

                ;
173426  012714          MOV     #163,(CSR)      ;Start the read

                ;
173432  105713          TSTB    (CTRL)          ;Finished?
173434  100376          BPL     .-2             ;No - wait
                ;
173436  121401          CMPB    (CSR),ONES      ;Read go OK?
173440  001401          BEQ     20$             ;Yes
                ;
173442                  MESSAGE SF              ;No - error message
                ;
173444  005007  20$:    CLR     PC              ;jump to zero
```


```
MT (TM11) MAGNETIC TAPE UNIT BOOTSTRAP
173446  012700  MTLOAD: MOV     #MTBRC,R0       ;Byte Count Register

173452  005310          DEC     (R0)            ;Get all primary boot block
173454  103422          BCS     RKLOAD          ;No Magtape controller - try RK
                ;
173456  032737          BIT     #100,@#MTS      ;Magtape On-line?


173464  001416          BEQ     RKLOAD          ;No, try RK
                ;
173466  012740          MOV     #60011,-(R0)    ;Space forward

                ;
173472  105710  10$:    TSTB    (R0)            ;Spacing finished?
173474  100376          BPL     10$             ;No - wait
                ;
173476  005710          TST     (R0)            ;Any errors?
173500  100407          BMI     MTERR           ;Yes
                ;
173502  012710          MOV     #60003,(R0)     ;Read in primary bootstrap

                ;
173506  105710  20$:    TSTB    (R0)            ;Read finished?
173510  100376          BPL     20$             ;No - wait
                ;
173512  005710          TST     (R0)            ;Any errors?
173514  100401          BMI     MTERR           ;Yes
                ;
                ;Primary Bootstrap read in. Execute it.
                ;
173516  005007          CLR     PC              ;Start it at ZERO
                ;
                ;I/O error
                ;
173520          MTERR:  MESSAGE MT              ;Error message and halt
```


```
RK (RK05) DISK BOOTSTRAP
173522  000241  RKLOAD: CLC                     ;Clear carry. It may be on
                                                ;if the system has no Magtape
                ;
173524  012700          MOV     #RKCSR,R0       ;Point at RK registers
                ;
173530  012720          MOV     #1,(R0)+        ;Reset Drive
173534  103435          BCS     NODEV           ;Can't - the Trap to 4
                                                ;indicates no RK controller
                ;
173536  012710          MOV     #-256.,(R0)     ;Set tranfer size
173542  012740          MOV     #5,-(R0)        ;Initiate read
                ;
173546  105710  10$:    TSTB    (R0)            ;Read finished?
173550  100376          BPL     10$             ;No - wait
                ;
173552  005710          TST     (R0)            ;Drive on-line?
173554  100762          BMI     RKLOAD          ;No - wait for it to come up
                ;
173556  005007          CLR     PC              ;Jump
                ;
```


```
                        ;
                        ;Trap Through 4 Dectector
                        ;
173560  052766  T4ADDR: BIS     #1,2(SP)        ;Just return with

                                                ;the Carry Bit set
173566  000002          RTI
                        ;
                        ;"TRAP" Message Routine.
                        ;
173570  011603  TRPADD: MOV     (SP),R3         ;Get trap pointer
173572  116303          MOVB    -2(R3),R3       ;And so get message pointer

173576  060703          ADD     PC,R3           ;Form message address
173600  062703          ADD     #<MESAGE-.>,R3

                        ;
173604  112737          MOVB    #'?,@#TXADATA   ;Error indicator out

                        ;
173612  105737  MESOUT: TSTB    @#TXACTL        ;OK to send next character?

173616  100375          BPL     MESOUT          ;No - wait
173620  112337          MOVB    (R3)+,@#TXADATA ;Character out

173624  001372          BNE     MESOUT          ;More?
                                                ;No
173626  000000          HALT
```


```
                        ;
173630                  NODEV:  MESSAGE NFW             ;No Boot Device Found
                        ;
173632                  MESAGE:
                        ;
173632  115             MEM:    .ASCIZ  /MEM/           ;Memory failure
  105
  115
  000
173636  104             DM:     .ASCIZ  /DM/            ;DM (Winchester) Boot Failure
  115
  000
173641  123             SF:     .ASCIZ  /SF/            ;Spectrum Floppy Boot failure
  106
  000
173644  115             MT:     .ASCIZ  /MT/            ;MT (Mag Tape) Boot Failure
  124
  000
173647  122             RK:     .ASCIZ  /RK/            ;RK  Cartridge Failure
  113
  000
173652  116             NFW:    .ASCIZ  /No Dev/        ;No boot device found.
  157
  040
  104
  145
  166
  000

                                .EVEN
                        ;
                        ;
                        ;Free Space
                        ;
        000114          MEMFREE =       BOOT+776-.
                        ;
                        ;Fill up remaining space
                        ;
        000046                  .REPT   BOOT+776-./2
                                .WORD   -1
                                .ENDR
                        ;
                        ;Version Number
                        ;
173776  030102                  .WORD   VERSION
```

BOOTSTRAP LISTING 2

```
                        ;
                        ;Initialization.
                        ;
                        .IF DF, $LIST$
000000                  .ASECT
        173000  .=173000                        ;For listing purposes only
                                                ;Code is completely relocatable
                        .ENDC
                        ;
173000                  YBBOOT:
173000                  BOOT::;
173000  000005          RESET                   ;Reset everything in case
                                                ;we were started from the
                                                ;console (via micro-ODT)
173002  012706          MOV     #1000,SP        ;Stack
                        ;
173006  012703          MOV     #ITSIZE,R3      ;Iterator size register
173012  012704          MOV     #ITFUNC,R4      ;Function (and, Read Only
                                                ;memory size)
173016  012705          MOV     #ITCSR,R5       ;Control and Status
```


```
173022                 MEMTEST:
173022  012737                 MOV     #-1,@#ITSADD    ;Memory set data


                       ;
                       ;
173030  011400                 MOV     (R4),R0         ;Get memory size
173032  012713         MINIT:  MOV     #140000,(R3)    ;32Kb to be initialized

173036  010702                 MOV     PC,R2
173040  000464                 BR      ITGO            ;Initialize memory to -1
173042  077005                 SOB     R0,MINIT        ;All done
                       ;
                       ;All memory set to -1
                       ;
                       ;Commence Well Test. This is done in 32Kb blocks,
                       ;because the memory size, in ITFUNC, is given in
                       ;number of 32Kb blocks.
                       ;
173044  011400                 MOV     (R4),R0         ;Get size of memory
                                                       ;in 32Kb blocks
                       ;
173046  005037                 CLR     @#ITDEXT        ;First block of memory

173052  012715                 MOV     #ITC$MF,(R5)    ;Indicate to Iterator that
                                                       ;Well test wanted

173056  012713         10$:    MOV     #140000,(R3)    ;32Kb to be tested.

                       ;
                       ;
173062  010702                 MOV     PC,R2
173064  000452                 BR      ITGO            ;Check it (?MEM error given
                                                       ;if failure detected)
173066  077005                 SOB     R0,10$          ;All Memory Tested?
                                                       ;Yes
                       ;
173070  004767                 JSR     PC,INTRAP       ;Set up trap vectors
```


DM (RK06/RK07 COMPATIBLE WINCHESTER) DISK BOOTSTRAP

```
                        ;
173074  012704  DMLOAD: MOV     #WCS1,CSR       ;Set up CSR address
                        ;
173100  012702          MOV     #100200,R2      ;Finished or end test for
                                                ;later
                        ;
173104  012714          MOV     #1,(CSR)        ;Select the drive
173110  103475          BCS     SFLOAD          ;No Winchester Controller
                                                ;exists
                        ;
173112  030214  10$:    BIT     R2,(CSR)        ;Select finished?
173114  001776          BEQ     10$             ;No - wait
                        ;
173116  005001          CLR     R1              ;Assume drive type is RK06
                        ;
173120  032737          BIT     #400,@#WDS      ;Drive RK06 or RK07?
173126  001402          BEQ     20$             ;RK06
                        ;
173130  012701          MOV     #2000,R1        ;Set type to RK07
                        ;
173134  012700  20$:    MOV     #100011,R0      ;Command: <ERROR RESET>
                                                ;<POWER UP> <GO>
173140  050100          BIS     R1,R0           ;Include drive type
173142  010014          MOV     R0,(CSR)        ;Issue command
                        ;
173144  030214  30$:    BIT     R2,(CSR)        ;Finished yet?
173146  001776          BEQ     30$             ;No - wait
173150  100413          BMI     DMLERR          ;Error - may be offline
                        ;
173152  012737          MOV     #-256.,@#WWC    ;1 Block transfer
173160  012700          MOV     #21,R0          ;Command: <READ> <GO>
173164  050100          BIS     R1,R0           ;Include Drive type
173166  010014          MOV     R0,(CSR)        ;Issue command
                        ;
173170  030214  40$:    BIT     R2,(CSR)        ;Primary Boot Read in yet?
173172  001776          BEQ     40$             ;No - wait
173174  100401          BMI     DMLERR          ;In Error
                        ;
173176  005007          CLR     PC              ;Tranfer execution to code
                                                ;just read in.
```


```
                        ;
173200  032737  DMLERR: BIT     #10000,@#WCS2   ;Winchester Off-line?

173206  001036          BNE     SFLOAD          ;Yes
                        ;
173210                  MESSAGE DM              ;No - Error Message
```


```
                        ;Start Iterator and wait for it to finish
                        ;
173212  012714  ITGO:   MOV     #ITF$MT,(R4)    ;Say 'GO'
                        ;
173216  105715  10$:    TSTB    (R5)            ;Finished Yet?
173220  100376           BPL     10$             ;No
                        ;
173222  005715           TST     (R5)            ;Test for parity error
173224  100404           BMI     MER
                        ;
173226  005713           TST     (R3)            ;Any data errors found?
                                                 ;(if there were, ITSIZE
                                                 ;would be non zero, which
                                                 ;when added to ITDADD &
                                                 ;ITDEXT points at the word
                                                 ;in error.
                                                 ;
173230  001002           BNE     MER             ;Error found. Very non-
                                                 ;structured but anything
                                                 ;goes in a Bootstrap.
                                                 ;
173232  000162           JMP     2(R2)

                        ;
                        ;Memory Test Failure
                        ;
173236  004767  MER:    JSR     PC,INTRAP       ;Initialize TRAP vectors

173242                   MESSAGE MEM
                        ;
                        ;Set up TRAP vectors
                        ;
173244  010701  INTRAP: MOV     PC,R1           ;Set up trap vectors
173246  062701           ADD     #<T4ADDRR-.>,R1

173252  012702           MOV     #4,R2           ;4 - Time out etc

173256  010122           MOV     R1,(R2)+        ;Trap pointer
173260  012712           MOV     #340,(R2)       ;And processor status
                        ;
173264  062701           ADD     #<TRPADD-T4ADDR>,R1

173270  012702           MOV     #34,R2          ;34-Trap instruction vector

173274  010122           MOV     R1,(R2)+        ;Vector address
173276  012712           MOV     #340,(R2)       ;And processor status

173302  000207           RTS     PC
```


```
                                        ;Set up Registers
                ;
173304          SFLOAD:
173304  012701          MOV     #-1,ONES

173310  012705          MOV     #SFSECT,SECT

173314  005015          CLR     (SECT)          ;Note:this instruction
                                                ;must be here, because
                                                ;the floppy disk controller
                                                ;chip,which this register is
                                                ;in,needs some time to repond.
                                                ;Therefore if CLR was
                                                ;immediately followed by the
                                                ;TST (below) the chip may
                                                ;not have time to repond
                                                ;correctly
                                                ;
173316  012702          MOV     #SFSEL,SEL

173322  012703          MOV     #SFCTRL,CTRL

173326  012704          MOV     #SFCSR,CSR

                ;
173332  005715          TST     (SECT)          ;Controller present?
173334  001050          BNE     MTLOAD          ;No - try the MT
                ;
                ; Wiggle all head motors to ensure track centering
                ;
173336  010012  WIGGLE: MOV     R0,(SEL)        ;Select Drive
173340  012714          MOV     #276,(CSR)      ;Step In

                ;
173344  105713          TSTB    (CTRL)          ;Finished?
173346  100376          BPL     .-2             ;No - wait
                ;
173350  012714          MOV     #236,(CSR)      ;Step out

                ;
173354  105713          TSTB    (CTRL)          ;Finished?
173356  100376          BPL     .-2             ;No - wait
                ;
173360  005200          INC     R0              ;Next drive
173362  042700          BIC     #177774,R0      ;Back to drive zero?

173366  001363          BNE     WIGGLE          ;No - wiggle this drive
                ;
173370  052700          BIS     #10,R0          ;Set double density bit.
```


```
                        ;
                        ;Now search for the first on-line drive
                        ;
173374                  DSEARCH:
173374  010012                  MOV     R0,(SEL)        ;Select drive
173376  105714                  TSTB    (CSR)           ;On-line?
173400  100405                  BMI     10$             ;Yes
                        ;
```


```
173402  005200          INC     R0              ;Select next drive
173404  032700          BIT     #4,R0           ;There can only be 4 drives

173410  001771          BEQ     DSEARCH         ;OK!
                ;
173412  000421          BR      MTLOAD          ;No SF floppies on line.
                                                ;Boot off the MT (if there
                                                ;is one)
                ;
                ;Boot off the on-line drive
                ;
173414  012714  10$:    MOV     #376,(CSR)      ;Home Seek

                ;
173420  105713          TSTB    (CTRL)          ;Finished?
173422  100376          BPL     .-2             ;No - wait
                ;
173424  012737          MOV     #-512.,@#SFSIZE ;512 byte transfer, into
                                                ;memory address zero
                ;
173432  010137          MOV     ONES,@#SFSECT   ;From sector zero

                ;
173436  012714          MOV     #163,(CSR)      ;Start the read

                ;
173442  105713          TSTB    (CTRL)          ;Finished?
173444  100376          BPL     .-2             ;No - wait
                ;
173446  121401          CMPB    (CSR),ONES      ;Read go OK?
173450  001401          BEQ     20$             ;Yes
                ;
173452                  MESSAGE SF              ;No - error message
                ;
173454  005007  20$:    CLR     PC              ;All is well, so jump to
                                                ;zero
```


```
173456  012700  MTLOAD: MOV     #MTBRC,R0       ;Byte Count Register
173462  005310          DEC     (R0)            ;Transfer all primary boot
                                                ;block
173464  103422          BCS     RKLOAD          ;No Magtape controller -
                                                ;try RK
                ;
173466  032737          BIT     #100,@#MTS      ;Magtape On-line?

173474  001416          BEQ     RKLOAD          ;No, try RK
                ;
173476  012740          MOV     #60011,-(R0)    ;Space forward
                ;
173502  105710  10$:    TSTB    (R0)            ;Spacing finished?
173504  100376          BPL     10$             ;No - wait
                ;
173506  005710          TST     (R0)            ;Any errors?
173510  100407          BMI     MTERR           ;Yes
                ;
173512  012710          MOV     #60003,(R0)     ;Read in primary bootstrap
                ;
173516  105710  20$:    TSTB    (R0)            ;Read finished?
173520  100376          BPL     20$             ;No - wait
                ;
173522  005710          TST     (R0)            ;Any errors?
173524  100401          BMI     MTERR           ;Yes
                ;
                ;Primary Bootstrap read in. Execute it.
                ;
173526  005007          CLR     PC              ;Start it at ZERO
                ;
                ;I/O error
                ;
173530          MTERR:  MESSAGE MT              ;Error message and halt
```


```
173532  000241  RKLOAD: CLC                     ;Clear carry. It may be
                                                ;on if the system has no
                                                ;Magtape
                ;
173534  012700          MOV     #RKCSR,R0       ;Point at RK registers
                ;
173540  012720          MOV     #1,(R0)+        ;Reset Drive
173544  103435          BCS     NODEV           ;Cannot - the Trap to 4
                                                ;detector indicates no RK
                                                ;controller
                ;
173546  012710          MOV     #-256.,(R0)     ;Set tranfer size
173552  012740          MOV     #5,-(R0)        ;Initiate read
                ;
173556  105710  10$:    TSTB    (R0)            ;Read finished?
173560  100376          BPL     10$             ;No - wait
                ;
173562  005710          TST     (R0)            ;Drive on-line?
173564  100762          BMI     RKLOAD          ;No - wait for it to come
                                                ;up
                ;
173566  005007          CLR     PC              ;Jump to block zero drive
                                                ;bootstrap
                ;
```


```
                        ;
                        ;Trap Through 4 Dectector
                        ;
173570  052766  T4ADDR: BIS     #1,2(SP)        ;Just return from the trap
                                                ;with the Carry Bit set
173576  000002         RTI
                        ;
                        ;"TRAP" Message Routine.
                        ;
173600  011603  TRPADD: MOV     (SP),R3         ;Get trap pointer
173602  116303         MOVB    -2(R3),R3       ;And so get message pointer

173606  060703         ADD     PC,R3           ;Form message address
173610  062703         ADD     #<MESAGE-.>,R3

                        ;
173614  112737         MOVB    #'?,@#TXADATA   ;Error indicator out


                        ;
173622  105737  MESOUT: TSTB    @#TXACTL        ;OK to send next character?

173626  100375         BPL     MESOUT          ;No - wait
173630  112337         MOVB    (R3)+,@#TXADATA ;Character out

173634  001372         BNE     MESOUT          ;More?
                                                ;No
173636  000000         HALT
```


```
173640                  NODEV:  MESSAGE NFW             ;No Boot Device Found
                        ;
173642                  MESAGE:
                        ;
173642      115         MEM:    .ASCIZ  /MEM/           ;Memory failure
   105
   115
   000
173646      104         DM:     .ASCIZ  /DM/            ;DM (Winchester) Boot Failure
   115
   000
173651      123         SF:     .ASCIZ  /SF/            ;Spectrum Floppy Boot failure
   106
   000
173654      115         MT:     .ASCIZ  /MT/            ;MT (Magnetic Tape) Boot
                                                        ;Failure
   124
   000
173657      122         RK:     .ASCIZ  /RK/            ;RK (archaic) Cartridge
                                                        ;Failure
   113
   000
173662      116         NFW:    .ASCIZ  /No Dev/        ;No boot device found.
   157
   040
   104
   145
   166
   000

                                .EVEN
                        ;
                        ;
                        ;Free Space
                        ;
            000104      MEMFREE =       BOOT+776-.
                        ;
                        ;Fill up remaining space
                        ;
            000042              .REPT   BOOT+776-./2
                                .WORD   -1
                                .ENDR
                        ;
                        ;Version Number
                        ;
173776      030102              .WORD   VERSION
```


1.1 SPECIFICATIONS

Identification	:	1538S
Size	:	Quad height
Dimensions	:	21.59cm x 26.68cm (10.5" x 8.5")
Power Requirements	:	3.5 amps at 5 volts
Bus Loads	:	1
Storage Environment	:	-40 deg C to 65 deg C
	:	10% to 90% relative humidity, non-condensing
Operating Environment	:	10 deg C to 38 deg C
	:	20% to 80% relative humidity, non-condensing

1.2 FEATURES

The features of the 'S' Board can be ascribed to:

the Sequencer (figure 1-1);
the CPU Handshake (figure 1-2);
the Register - Arithmetic/Logic Unit (figure 1-3);
the Memory System (figure 1-4);
the Iterator (figure 1-5).

SEQUENCER

The principle element of the GPMI is a 68-bit 512 word microprogrammed controller cycling at 125 nanoseconds, with it's address space being logically organized as 256 odd/even pairs.

At each step of the microsequence, a jump can be made to any address pair location via the 'next address' PROM. The allocation of odd or even to a target location is determined by the micro address bus zero value which is generated by the 'branch condition multiplexer'. This can be unconditionally odd or even or else a conditional branch can be taken on the value of any of the remaining 6 states throughout the system; these normally being ALU condition bits.

The 'next address' and 'branch condition multiplexer' PROMS account for 12 bits of microcode while the remaining 56 bits hang off this micro address bus and control all the various bus gates, ALU functions and device control enables and clocks, throughout the system.

At the completion of each micro-sequence, 'enable next address' is released with one of the upper two PROMS being enabled to determine the prioritized start address for the next pending operation.

The upper PROM maps the CPU and Q-Bus requests into a dedicated set of routines to service such operations as -

Memory deposit
Bootstrap read
Character output to VDU

The middle PROM maps local service operations such as -

Memory refresh
Floppy disk DMA read transfer
Winchester disk DMA write transfer
Device interrupt request

As each routine is entered, the 'next address' PROM takes over until completion of that function.

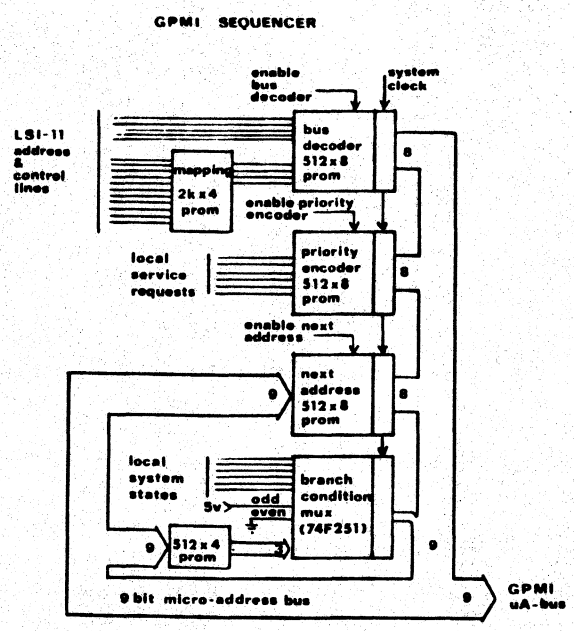


Figure 1-1

CPU HANDSHAKE

When the CPU makes a request for memory or I/O device access, it raises the applicable bus signal DIN (input data) or DOUT (output data). This signal then arms the D Flip-Flop to enable the bus decoder and disable the priority encoder at the next end-of-sequence as released by the microprogram.

To illustrate: upon entry to the bus request service routine, it is already known (through mapping) that a byte is to be deposited to the line printer. At a suitable point in this dedicated routine, a pulse is supplied to the NOR gate flip-flop and a BUS REPLY is generated. The GPMI is then free to enter internal housekeeping routines while the CPU completes the bus handshake in its own time. (DOUT eventually drops, resetting REPLY).

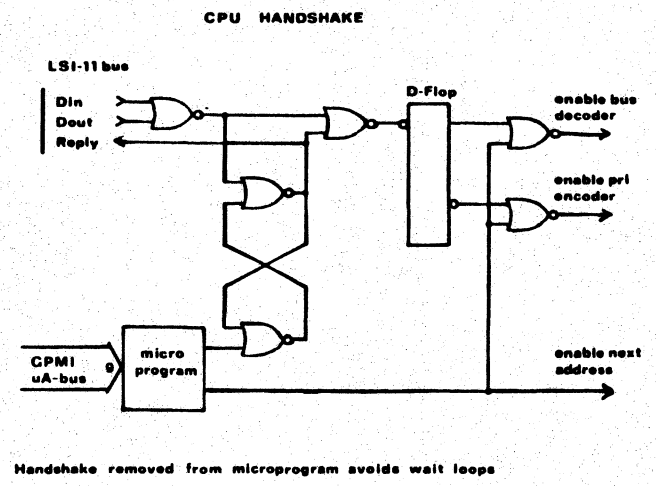


Figure 1-2

REGISTER & ARITHMETIC/LOGIC UNIT

On board memory for the GPMI is fixed at 1 megabyte which requires 20 address bits. As on board DMA is carried out, several 20-bit address values must be stored for concurrent operations where fast arithmetic, ie., increment at least, processing can be performed as the transfers progress.

This processing is achieved by a 20-bit RALU using 5 X 2903 4-bit slices, and external carry-lookahead methods are used to maintain the same rate as the 8MHz sequencer. The RALU drives the address bus alternatively with the Q-bus.

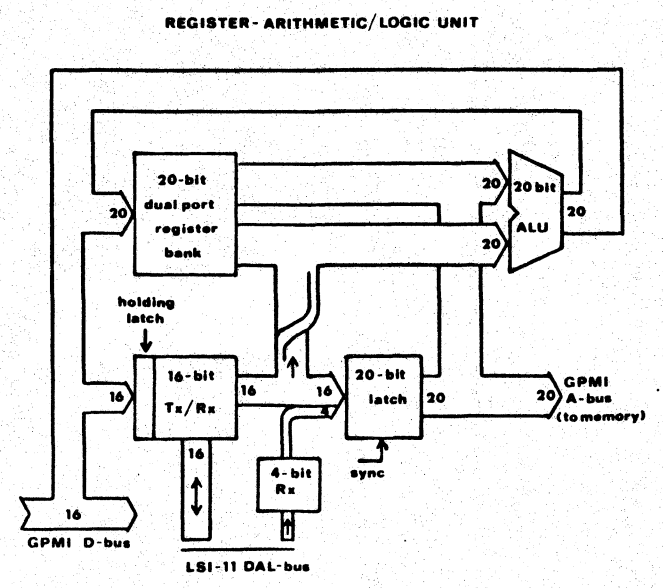


Figure 1-3

As well as performing address arithmetic and while in the process of operating on the I/O devices, the RALU is used with data to: CLEAR, ROTATE, COMPLEMENT, AND, OR, COMPARE, GENERATE CONSTANTS, and MAINTAIN WORD COUNTS.

MEMORY SYSTEM

The address bus is generated to look up locations either in RAM, read/write memory or, in the read only bootstrap (initial program load executed on power up).

The memory chips used are either 16K X 1 bits or 64K X 1 bits, with the design expandable to allow 256K X 1 bit chips when these are released on the market.

These chips are conceptually 2-dimensional arrays which need initially, a row address and then a column address dispensed over the same lines. At 2 millisecond intervals, every row of every array is refreshed by cycling memory at that address. This is organized as a background task for the GPMI via an interval timer fed into the priority encoder.

As this form of memory is volatile, the design allows for an optional battery which powers memory only in the event of a power fail. If power is lost while the mains switch is on, the memory array then receives current from the 5-volt battery which is physically mounted outside the processor unit. The processor takes a power fail trap, executes a routine to save the CPU registers in memory and then operates a microcode signal referred to as STORE. This in turn pulls down Pin 1 of all RAMS and they enter a self-refresh state. Two transistors are connected to form a flip-flop which holds the logical state until the battery itself fails.

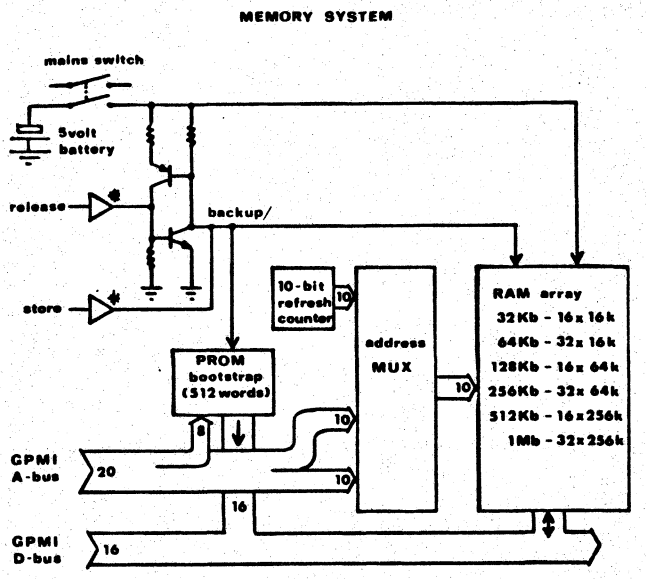


Figure 1-4

When power is restored, the normal bootstrapping process flips to the second page which constitutes a totally different botstrap routine. Where page one carries out destructive memory tests and system load, page two simply enables the RELEASE line and jumps to a routine in memory which restores the CPU registers. Processing then continues as though an interrupt has not occurred.

ITERATOR

Within the GPMI hardware and without implementing any additional hardware, there exists a means by which a number of useful iterative memory operations can be implemented.

These operations include the facility whereby -

a block of data can be moved from one area of memory to another, in either direction;

memory initialize and memory test functions can be carried out.

Three of the spare 20-bit registers from the Register bank in the GPMI microsequencer (refer RALU) have been assigned (with the appropriate microcode) to perform the above functions. These registers , commonly defined as an Iterator, have been assigned Q-bus addresses and are therefore accessible to the LSI-11 for initialization. These three registers are -

Iterative Source Address (20 bits)
Iterative Destination Address (20 bits)
Iterative Transfer Count (16 bits)

The remaining 4 bits of the Transfer Count Register are allocated to the Iterative Function Register.

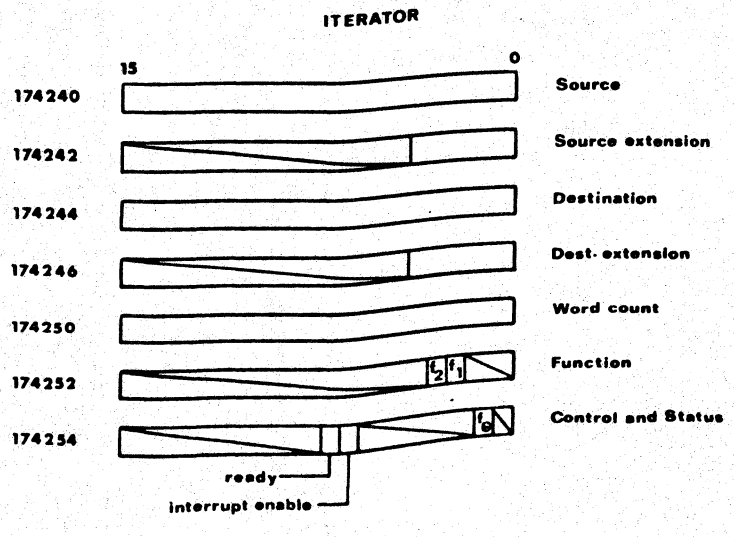


Figure 1-5

As the Iterator is actioned as an I/O device, the mandatory requirement of a Control and Status Register is implemented. This contains a ready bit and an interrupt bit. The LSI-11 processor instructs the Function Register as to which operation is to be performed; thus starting the operation.

The block move function of the Iterator can be used to emulate the activity of a disk for user swapping and program overlaying although at a far greater speed than a disk.

The memory initialization and memory test functions are invoked during the automatic bootstrap procedure to verify memory integrity.

Any of the operations, as detailed above, can be executed by the Iterator at a far greater speed than if performed by the LSI-11 itself. This is because -

no instructions are needed for fetch and decode;
no CPU or bus delays occur due to intimate memory access;
the LSI-11 processor continues other tasks in parallel.

2.1 SPECIFICATIONS

Identification	:	1538M,1538B
Size	:	Quad height
Dimensions	:	25.5cm x 19.8cm (10" x 7.8")
Power Requirements	:	3.5 amps at 5 volts
Bus Loads	:	Nil
Storage Environment	:	-40 deg C to 65 deg C
	:	10% to 90% relative humidity, non condensing
Operating Environment	:	10 deg C to 38 deg C
	:	20% to 80% relative humidity, non-condensing

2.2 FEATURES

The features of the 'B/M' Board can be ascribed to:

the selected I/O Devices (figure 2-1);
the Interrupt Processor (figure 2-2).

2.2.1 Selected I/O Devices

It is at this juncture that clarification of the 'B' and 'M' Board is required. Some of the I/O devices that the 'B' board has control of, vary from those under the control of the 'M' Board, while all other elements remain identical. This chapter defines the philosophy of both boards.

'M' BOARD	'B' BOARD
2 Serial Lines	2 Serial Lines
1 Line Printer	1 Line Printer
	1 Card Reader
Up to 4 Floppy Disk Drives - using double sided/double density diskettes (maximum storage 5Mb)	Up to 4 Floppy Disk Drives - using single sided/single density diskettes (maximum storage 1.2Mb)

I/O DEVICES

As the Spectrum Eleven GPMI was designed to meet the requirements of various types of applications, the I/O device distribution was planned in accordance with this.

The I/O devices selected for this interface suffice for small business, laboratory, industrial and educational purposes, with the system expandable to include a secondary specialized I/O processor which handles up to 260Mb of Winchester disk.

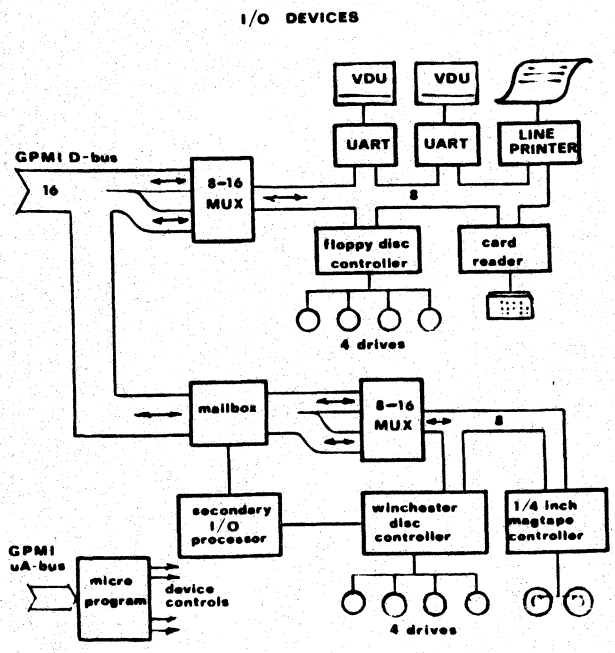


Figure 2-1

The devices are linked to a bidirectional data bus and controlled directly with 56 bits of microprogram (the 'next address' and 'branch condition multiplexer' PROMS account for the other 12 of the 68 bits).

Each device has its own peculiar addressing, clocking, and handshaking scheme; all of which are handled by the micro sequencer as a series of microprogrammed steps.

INTERRUPT PROCESSOR

As each I/O device on the system completes a task set originally by the CPU, an associated READY bit is set by the device.

The task could be -

A character is to be serialized and sent to a terminal screen;
A character is to be received from a terminal keyboard;
A block of data is to be received from the floppy disk and placed in memory.

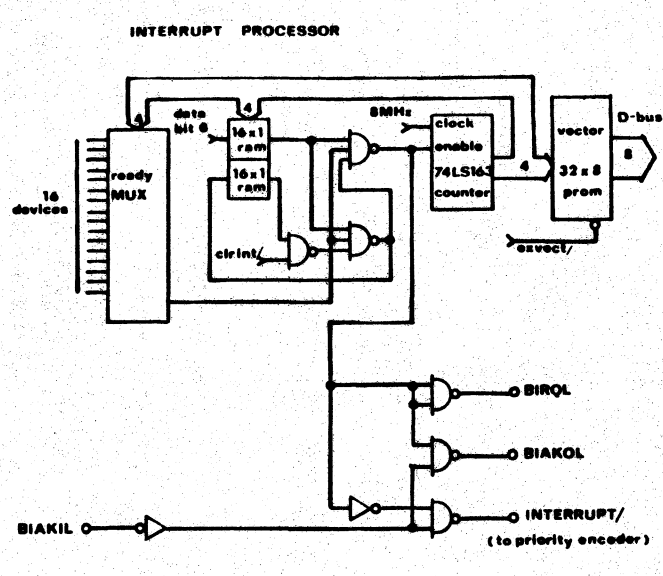


Figure 2-2

These READY bits are multiplexed down to a single READY line which can be used to interrupt the CPU. The CPU stops its current task and asynchronously and immediately provides service to the interrupting device(s), and on completion of this service resumes the original task.

This function can be turned on or off by means of an 'interrupt enable' bit associated with each READY bit. The GPMI allows a maximum of 16 READY/ENABLE pairs which have been implemented

respectively as a 16-bit multiplexer and a 16-bit RAM. These READY/ENABLE pairs are polled in a round-robin fashion at 8MHz by a 74LS163 counter and tested by a 7410 gate. When an enabled device becomes ready:

1. The counter stops;
2. The CPU is informed by an interrupt request;
3. The vector (service request address for service) is made ready.

When the CPU is ready, it replys via BIAKIL which generates signal INTERRUPT. This causes the GPMI sequencer to enter a service routine which completes the interrupt cycle by placing the appropriate vector on the Q-Bus to be read by the CPU (via EXVECT) and subsequently enables the counter (via CLRINT) to continue its round robin scanning process.

Once an interrupt cycle has been activated, a 'service' bit becomes set in a second 16-bit RAM, and all subsequent identical interrupt requests are ignored until the original process is complete. When a new task commences, the READY line goes low and the 'source' bit is reset. This process inhibits repeated interrupts from the same event.

3.1 SPECIFICATIONS

Identification	:	1538T
Size	:	Quad height
Dimensions	:	21.59cm x 26.68cm (10.5" x 8.5")
Power Requirements	:	3.5 amps at 5 volts
Bus Loads	:	Nil
Storage Environment	:	-40 deg C to 65 deg C
	:	10% to 90% relative humidity, non-condensing
Operating Environment	:	10 deg C to 38 deg C
	:	20% to 80% relative humidity, non-condensing

3.2 FEATURES

A Winchester disk controller comprised of -

the Sequencer (figure 3-1);
the Register & Arithmetic/Logic Unit (figure 3-2);
the Mail Box (figure 3-3);
the Silo (figure 3-4);
the Serial Sequencer (figure 3-5).

SEQUENCER

This sequencer operates synchronously with the sequencer on the 'S' board and functions in the same manner although certain differences require a mention.

There is only one mapping PROM which determines the prioritized start address, whereas on the 'S' board there are two;

Conditional branches can be taken on the value of any of 30 states within the 'T' board.

The sequencer performs the following functions -

it simulates the RK07 register set;

in conjunction with the 'S' board sequencer, it controls data transfers between disk and memory;

it re-maps RK07 disk addresses into disk addresses suitable for the particular drive connected;

it decodes and initiates the disk commands requested by the CPU.

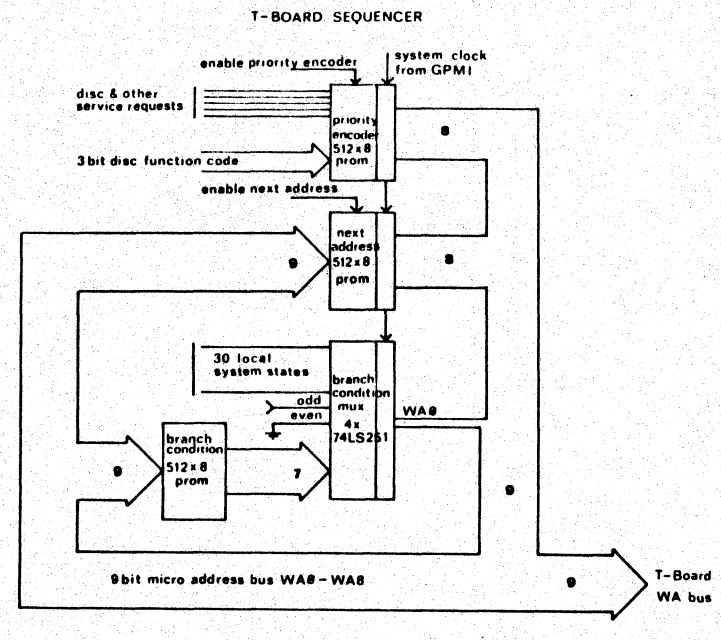


Figure 3-1

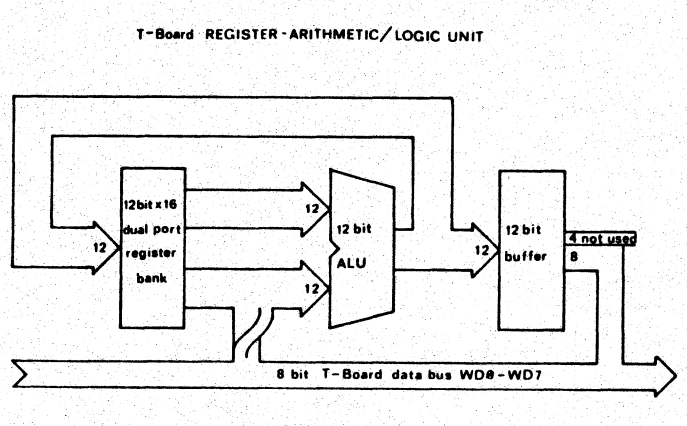


Figure 3-2

REGISTER & ARITHMETIC/LOGIC UNIT

All arithmetic processing is performed within a 12-bit wide RALU. This width was chosen to encompass the largest binary number required to be processed. The RALU consisting of 3 X 2901 4-bit slices is controlled by the sequencer.

The register set is used for storing current values of disk addresses, temporary processing values, etc.

MAIL BOX

The Mail box provides the only communication link between the 'S' board and the 'T' board. It consists of a bank of sixteen 16-bit registers with these registers being accessible by both sequencers.

To prevent simultaneous access by both sequencers, the 'S' board sequencer is gadort which then forces the 'T' board sequencer to wait until the 'S' board no longer requires the use of the mail box.

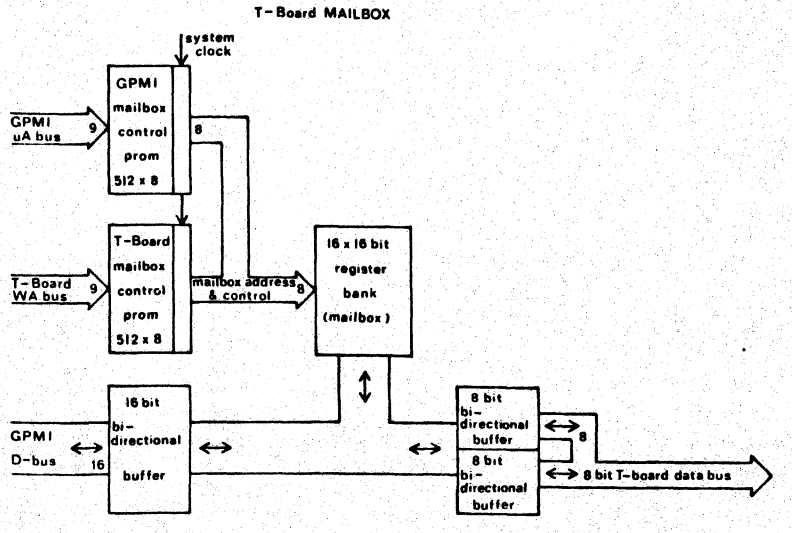


Figure 3-3

The majority of these registers have been defined as the RK07 register set although one is used as a buffer for data transfers and the remaining few have been reserved for future use.

A simple handshaking scheme is implemented so that access to the Mail Box can be controlled.

SILO

The silo acts as a data buffer between the disk and the memory and performs the function of serial to parallel conversion when reading from disk or parallel to serial when writing to disk.

It consists of a stack of sixteen 8-bit registers providing sufficient buffering of disk data to prevent data overrun problems.

At the serial interface of the silo (the disk connection), data is transferred at the disk clock rate to meet the requirements of the disk.

At the parallel interface of the silo (the T-board sequencer connection), data is transferred at the system clock rate (8 MHz).

The silo provides elasticity and short term independence of these opposing requirements.

T-Board SILO

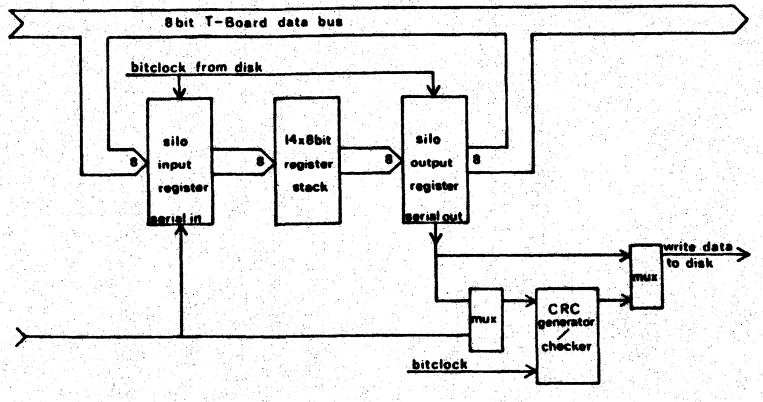


Figure 3-4

SERIAL SEQUENCER

This sequencer provides a set of signals which control the disk drive, the silo, and the CRC circuit, during the transfer of a block (512 bytes) of disk data. It also provides byte synchronisation to serial disk data (during read operations) and status information to the controller, ie., Header Done, Sector Done.

The serial sequencer consists of a counter which is initialized at the beginning of a sector and is clocked at the disk rate. Consequently this counter keeps track of the position within a disk sector. The outputs of the counter along with a function code, are decoded by two 2K x 8 PROMS to provide the required control signals.

T-Board Serial Sequencer

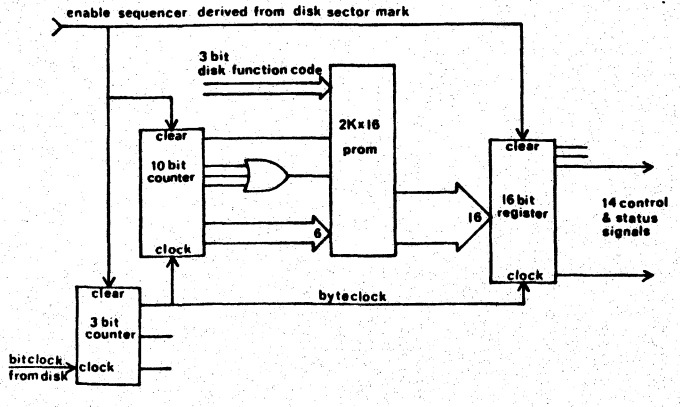


Figure 3-5

TYPE II
m = Multiple Record flag (Bit 4) m=0, Single record m=1, Multiple Records b = Block length flag (Bit 3) b=1, IBM format (128 to 1024 bytes) b=0, Non-IBM format (16 to 4096 bytes) E = Enable HLD and 10 msec Delay (Bit 2) E=1, Enable HLD,HLT and 10 msec delay E=0, Head is assumed Engaged and there is no 10 msec delay a1a0 = Data Address Mark (Bits 1-0) a1a0 = 00,FB (Data Mark) a1a0 = 01,FA (User defined) a1a0 = 10,F9 (User defined) a1a0 = 11,F8 (Deleted Data Mark)

TABLE 9-3

TYPE III
s/ = Synchronize flag (Bit 0) s/=0, Synchronize to AM s/=1, Do not synchronize to AM

TABLE 9-4

TYPE IV
Ii = Interrupt Condition flags (Bits 3-0) I0 = 1, Not Ready to Ready Transition I1 = 1, Ready to Not Ready Transition I2 = 1, Index Pulse I3 = 1, Immediate Interrupt

TABLE 9-5

Stepping Rates

The four programmable stepping rates (Table 9-6) can be applied to a Step-Direction Motor through the device interface.

Step

A 2 ns pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)

The direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12ns before the first stepping pulse is generated.

When a Seek, Step or Restore command is executed, an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millesecond settling time after the head is loaded against the media. The track number from the first encountered ID field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is preset.

CLK / DDEN / r1 r0	2 MHz 0 TEST/=1	1 MHz 1 TEST/=1	1 MHz 0 TEST/=1	1/2 MHz 1 TEST/=1	2 MHz TEST/=0	1 MHz TEST/=0
0 0	3ms	3ms	6ms	6ms	Approx. 400 ns	Approx. 800 ns
0 1	6ms	6ms	12ms	12ms		
1 0	10ms	10ms	20ms	20ms		
1 1	20ms	20ms	40ms	40ms		

TABLE 9-6

The Head Load (HLD) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E flag On) or Verify operation, or a Seek or Step operation with the head load bit, h, a logic one, and remains activated until the third index pulse following the last operation which used the read/write head. Reading or writing does not occur until a minimum 10 msec delay after the HDL signal is made active. If executing the Type II commands with the E flag off, there is no